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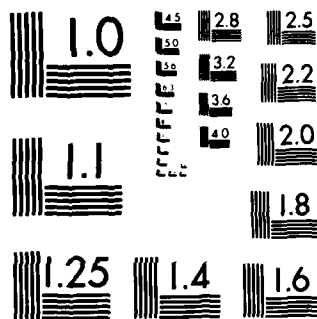
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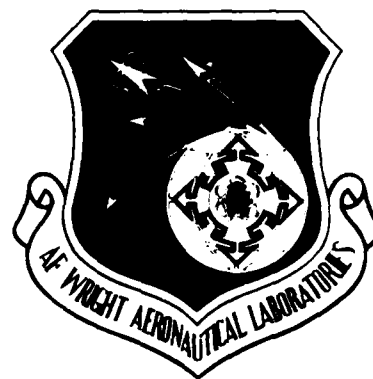
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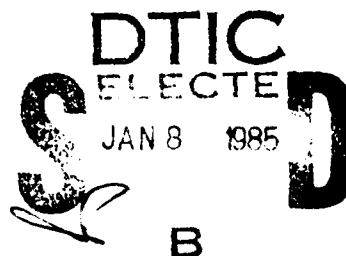
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July 1984

Interim Report for Period October 1982 - October 1983

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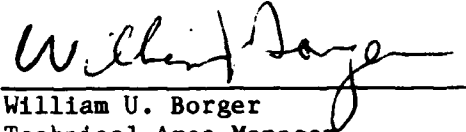
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This technical report has been reviewed and is approved for publication.



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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM								
1. REPORT NUMBER AFWAL-TR-84-2047	2. GOVT ACCESSION NO. A149335	3. RECIPIENT'S CATALOG NUMBER								
4. TITLE (and Subtitle) ADVANCED INVERTER TECHNOLOGY		5. TYPE OF REPORT & PERIOD COVERED Interim Report for Oct 1982 to Oct 1983								
7. AUTHOR(s) R. L. Moser		6. PERFORMING ORG. REPORT NUMBER MCR-83-644								
9. PERFORMING ORGANIZATION NAME AND ADDRESS Martin Marietta P. O. Box 179 Denver, CO 80201		8. CONTRACT OR GRANT NUMBER(s) F33615-82-C-2239								
11. CONTROLLING OFFICE NAME AND ADDRESS Aero Propulsion Laboratory (AFWAL/POOS) Air Force Wright Aeronautical Laboratories (AFSC) Wright-Patterson Air Force Base, Ohio 45433		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS Project 3145 Task 32 P.E. 62203F W.U. 72								
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)		12. REPORT DATE July 1984								
		13. NUMBER OF PAGES 71								
		15. SECURITY CLASS. (of this report) Unclassified								
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE								
16. DISTRIBUTION STATEMENT (of this Report) Approved for public release; distribution unlimited.										
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)										
18. SUPPLEMENTARY NOTES										
19. SUBJECT TERMS (Continue on reverse side if necessary and identify by block number) Control Architecture Generalized SRI Control and Protection Converter Control Power Converter Converter Protection Series Resonant Inverter Control Gate Control (SCR)										
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) This report gives the results of the Phase I Study Tasks for the Advanced Inverter Technology program. APL has three existing series resonant inverter-based power converters: <table border="0"> <tr> <td>Power --</td> <td>Topology --</td> </tr> <tr> <td>10 kW</td> <td>dc/dc 1/2 Bridge,</td> </tr> <tr> <td>5 kW</td> <td>ac/dc Full Bridge,</td> </tr> <tr> <td>200 kW</td> <td>dc/dc Dual Full Bridge,</td> </tr> </table>			Power --	Topology --	10 kW	dc/dc 1/2 Bridge,	5 kW	ac/dc Full Bridge,	200 kW	dc/dc Dual Full Bridge,
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5 kW	ac/dc Full Bridge,									
200 kW	dc/dc Dual Full Bridge,									

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20. ABSTRACT (Continued)

The control and protection circuits are different for the three units. The purpose of this program was to produce a control and protection architecture and functional circuits that would work with all three power stage topologies. The requirements for the three existing power stages were determined. The three existing control and protection circuits were analyzed. An IC technology study was performed to determine the optimum technology and fabrication method for SRI control and protection circuits. A control and protection architecture utilizing common functional circuits that would work with the three existing topologies was developed and block diagrams drawn. The functional tasks were partitioned into five custom parts. The requirements for the custom parts were described. A study was performed to assess the potential present and future functions for a microprocessor in a series resonant inverter. A packaging and thermal study was performed to investigate the problems associated with space deployment of a 200-kW series resonant inverter. Recommendations for control and protection architecture, functional circuits, parts selection, and fabrication as hybrid circuits are made.

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FOREWORD

This Martin Marietta Denver Aerospace Interim Report covers the Phase I work accomplished on Contract F33615-82-C-2239 for the period of October 1982 to October 1983.

This contract is being performed for the Aero Propulsion Laboratory, Air Force Wright Aeronautical Laboratories, Air Force Systems Command, Wright-Patterson AFB, Ohio. The program is under the technical direction of Michael Dougherty, AFWAL/POOS-2.

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ACRYONYMS AND ABBREVIATIONS

A	Anode
ac	Alternating Current
All	Advanced Inverter Technology
ALU	Arithmetic Logic Unit
APL	Aero Propulsion Laboratory
BB	Breadboard
BBS	Back-Bias Sensor
CU	Control Unit
CMOS	Complimentary Metal Oxide Semiconductor
CMOS/SOS	CMOS/Silicon on Sapphire
CRM	Center for Radiation Hard Microelectronics, Sandia National Laboratories
dc	Direct Current
DI	Dielectric Isolation
ECL	Emitter-Coupled Logic
FF	Flip-Flop
FPG	Firing Pulse Generator
G	Gate
GFP	Government-Furnished Property
GPU	General Processing Unit
GUA	Gate Universal Array
IC	Integrated Circuit
IG	Gate Current
I ² L	Integrated Injection Logic
K	Cathode of SCR
kW	Kilowatts
LSI	Large-Scale Integration
LSTTL	Low-Power Schottky Transistor Transistor Logic
MSI	Medium-Scale Integration
NMOS	Negative Metal Oxide Semiconductor
Pa-cm	PASCAL - Centimeter
PMOS	Positive Metal Oxide Semiconductor
PU	Protection Unit
Rad (Si)	Radiation Silicon
RFT	Request for Transition

ACRYONYMS AND ABBREVIATIONS (concl)

SCR	Silicon-Controlled Rectifier
SFT	Safe for Transition
SOS	Silicon on Sapphire
SSI	Small-Scale Integration
TQ	SCR Reverse Recovery Time
TTL	Transistor-Transistor Logic
UPS	Uninterruptible Power Source
WPAFB	Wright Patterson Air Force Base

1.0 BACKGROUND

1.1 INTRODUCTION

Several different series-resonant-inverter-(SRI)-based converters have been developed for the Aero Propulsion Laboratory (APL) of Wright Patterson Air Force Base (WPAFB) over the years. The control and protection circuits for these converters varied and were built of discrete components. This program was established to simplify and standardize the control and protection circuitry and to use modern integrated circuit (IC) technology to reduce the converter's size.

This interim report covers the work accomplished during the period from October 1982 to October 1983.

1.2 OBJECTIVES

The primary objective of this program is to develop a standardized control and protection circuit that will work with any SRI-based converter; a hybrid implementation version of the control and protection circuitry will be produced. The secondary objective is to identify potential problem areas associated with using the existing 200-kW dual full-bridge SRI in space.

1.3 SCOPE

The scope of this program is limited to control and protection circuitry for an SRI-based converter including analysis of the operation of the control and protection circuitry for the three existing APL converters. It includes recommending approaches to reduce the size and complexity of the control and protection circuitry through IC technology. The program includes design, fabrication, and test of a breadboard and a prototype of the standard control and protection circuitry. Operation of the standard control and protection circuitry will be demonstrated with the three existing APL power stages.

1.4 PHASE I TASKS AND SUMMARY OF KEY RESULTS

1.4.1 Converter Requirements Definition

The objective of this task was to define the requirements and interfaces for the three specified APL converters. The converter

requirements for the three specified APL converters have been collected in a requirements document. The electrical inputs and outputs, as well as details of the interfaces between the controller and the three power stages, have been incorporated in this document. The primary objective of this program is to develop a set of standardized control and protection modules that can be configured to control any SRI topology. This controller will provide a voltage regulator output characteristic that will operate from 10% of rated load to rated load. Input and output overvoltage protection will be provided and the control and protection units will operate with an output transformer or a short for testing.

1.4.2 Control and Protection Analysis

The objective of this task was to analyze the implementation and requirements for the control and protection circuits for the three existing SRI-based converters. The 5-kW ac-dc and 10-kW dc-dc units were government-furnished property (GFP) to Martin Marietta at Denver. Analysis and operation of these units, as well as analysis of the 200-kW dc-dc unit which remained at WPAFB, revealed unique requirements and previously unknown details of control and protection circuit operation. In addition, electrical schematics were prepared for the complete 10-kW unit, all the control boards of the 200-kW unit, and selected parts of the 5-kW unit. Through this a detailed understanding of the operation and performance requirements for the control and protection circuits has resulted.

Analysis of the 5-kW ac-dc unit revealed two unit requirements. Back-bias sensors (BBS) for this unit must tolerate ac voltage and not saturate. There is also a requirement for the protection unit to prevent simultaneous conduction of series SCRs during phase transition. Analysis of the 10-kW dc-dc unit uncovered an unreported inversion in the control integrator and an unreported use of the resonant capacitor voltage in the control and protection implementation. A detailed understanding of the operation and requirements for control and protection was acquired from analyzing and operating the 10-kW dc-dc unit. Analysis of the 200-kW dc-dc unit revealed a non-resetting integrator in the controller.

1.4.3 IC Technology Study

The objective of this study was to identify process and fabrication IC technologies for implementing the control and protection circuits. For the near term, it is practical to design for 10^5 rad (SI). Test data are available to substantiate this level of radiation tolerance and parts are available from manufacturers. If the background level is greater than this, local shielding must be used to reduce the piece-part radiation level to 10^5 rad (SI). The following recommendations are made for the control and protection circuits: (1) digital circuits should be CD40XX series CMOS (2) IC operational amplifiers and voltage comparators should be bipolar monolithic LM108s and LM111s (3) the digital design constraints of the Sandia Center for Radiation-Hardened Microelectronics (CRM) should be followed (4) hybrid circuit technology should be used for the firing pulse generator (FPS), BBS, protection unit (PU), and three-phase unit and (5) discrete circuits should be used for the control circuit.

1.4.4 Functional Design

In the functional design task, all of the required functions of the control and protection circuits were identified, duplicate functions were identified and removed, the identified functions were partitioned to logical groupings of functional circuits, all signals associated with each circuit were identified, and block diagrams of the control and protection circuits that interface with each of the three existing APL power stages were developed.

1.4.5 Custom Part Specifications

The objective of this task was to define the custom part specifications. The control and protection functions were partitioned into five areas and custom part specifications were written for the following five parts:

- 1) Back-bias sensor (BBS);
- 2) Firing pulse generator (FPG);
- 3) Protection unit (PU);
- 4) Three-phase unit (TPU);
- 5) Control unit (CU).

The custom parts specifications have a narrative description of the requirements, both top-level and detail requirements, a block diagram, a circuit schematic, power requirements, and a parts list.

1.4.6 Microprocessor Study

There were two purposes for the microprocessor study. The first was to consider using a microprocessor to reconfigure the control and protection circuitry for the three existing power stages. The second was to identify tasks that could be performed by a microprocessor on future SRIs.

The study concluded that a microprocessor is not appropriate to reconfigure the controller to the three existing APL power stages because the reconfiguration can simply be performed by a three-position rotary switch. If a microprocessor were used, an uninterruptible power source (UPS) would be required, and a microprocessor malfunction could cause unknown damage to a power stage. It was also determined that a microprocessor was too slow for use as an embedded controller. The control and protection functions can be performed much faster by dedicated analog and digital circuits.

Several candidate microprocessor functions for future SRIs were identified, however. These functions can be performed either by a local microprocessor in the SRI or by a central microprocessor in the electrical power subsystem. These candidate functions are:

- 1) Data acquisition;
- 2) Limit checking;
- 3) Self-protection;
- 4) Monitor key parameters;
- 5) Efficiency calculation;
- 6) State of health monitoring;
- 7) Peak power tracking with solar array.

1.4.7 Thermal Study

The purpose of the thermal study was to provide a first-order assessment of the magnitude of the problems associated with space deployment of the 200-kW SRI. From this study it was determined that the SCR-diode pair effectively sets the radiator temperature. The most likely radiator temperature would be constrained at about 57°C when power semiconductor junction temperatures are at 125°C maximum. To limit the SCR temperatures, heat pipes are recommended. Under ideal conditions to keep a radiator at 57°C, the radiator area would be 150 ft² to reject 8 kW thermal from the 200-kW SRI. This study assumed ideal conditions. For systems not under ideal conditions, the radiator area would be significantly larger.

1.4.8 Packaging Study

The general packaging problems associated with space deployment of the 200-kW SRI were addressed. The study was limited to the low-voltage power stage only; the high-voltage output transformer, rectifiers, and capacitor were excluded. The study, which assumed ideal conditions, revealed no insurmountable packaging problems with space deployment of the 200-kW SRI. The projected weight of a 200-kW converter unit (including the power electronics, thermal control, and radiator) was 339 lb for a specific weight of 1.7 lb/kW. For a system with nonideal conditions, the specific weight will be significantly higher.

2.0 PHASE I STUDY TASKS

2.1 CONVERTER REQUIREMENTS DEFINITION

2.1.1 Top-Level Requirements

The standard control and protection circuitry will perform the functions necessary to start, operate, regulate, protect, and shut down an SRI-based converter. The controller is required to work with any SRI-based converter topology, and with either ac-dc or dc-dc converters. The controller will mechanize a voltage regulator function.

2.1.2 Target SRI-Based Converters

The standard controller will be designed to work with the following three existing APL SRI-based converters. By reconfiguring one controller design it will be able to operate each of the three converters.

Table 2.1-1 describes the three existing APL SRI-based converters. Simplified schematics of the power stages for these devices are shown in Figures 2.1-1 through 2.1-3 (Ref 1, 2, and 3).

Table 2.1-1 SRI Power Converter Characteristics

Type	Power	V (In)	V (Out)	Topology
ac-dc	5 kW	208 Vdc 3-Phase	20 kV dc	3-Phase ac Full Bridge
dc-dc	10 kW	600 Vdc Max	10 kV dc	1/2 Bridge
dc-dc	200 kW	600 Vdc Max	25 kV dc	Twin Full Bridge

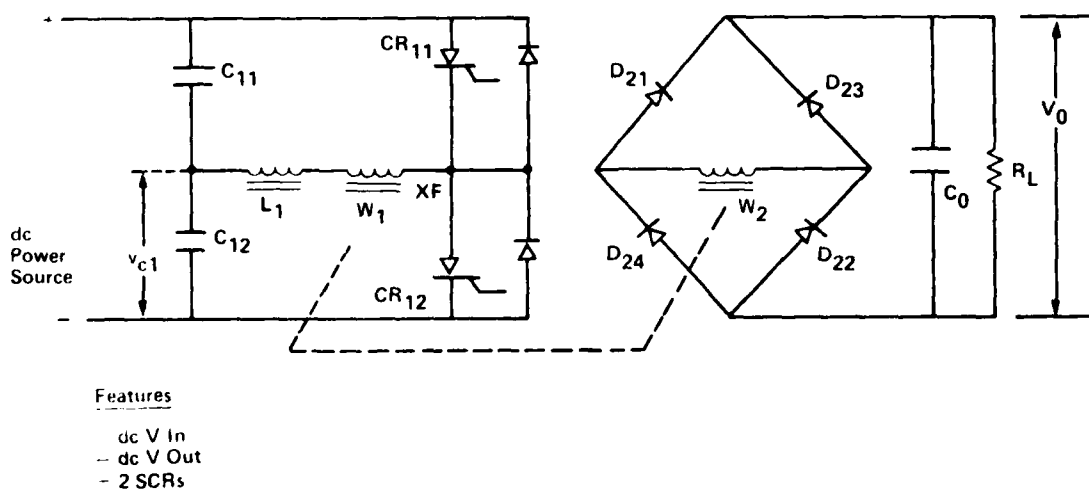


Figure 2.1-1 Half-Bridge SRI-Based Converter—10-kW dc-dc

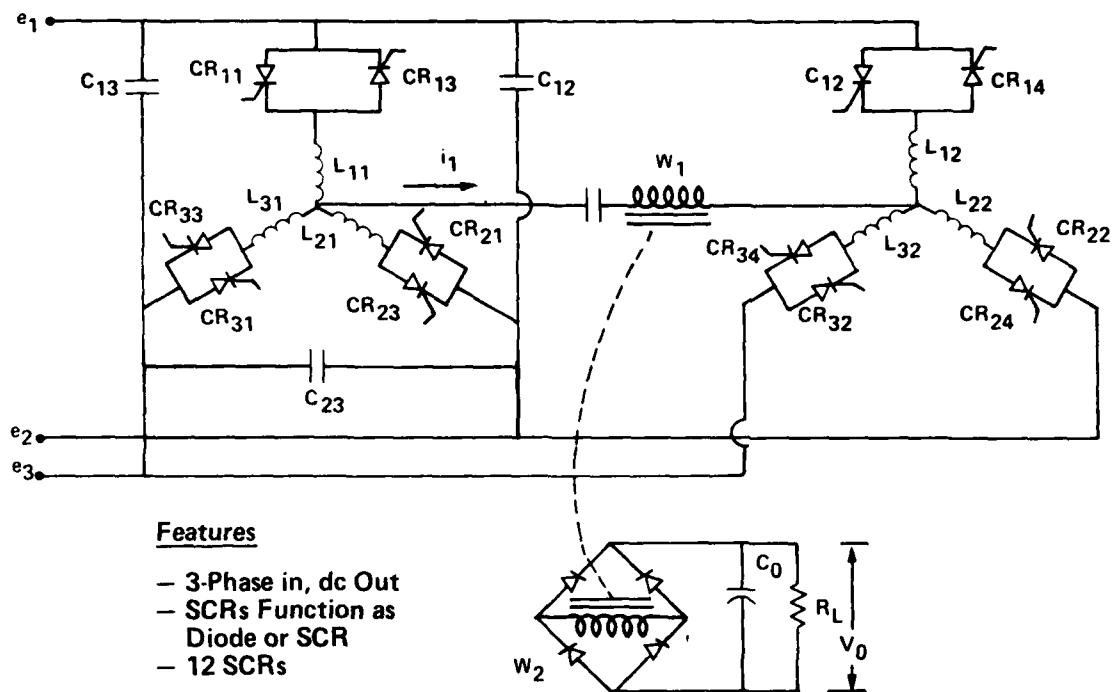


Figure 2.1-2 Three-Phase ac-dc/SRI-Based Converter-5-kW ac-dc

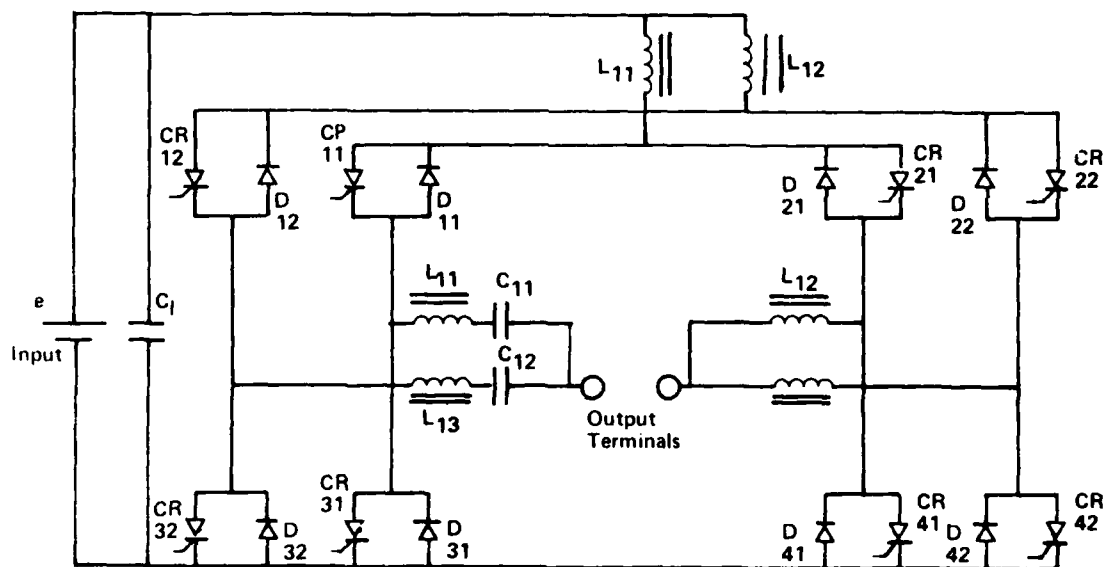


Figure 2.1-3 200-kW dc-dc, Dual, Full-Bridge SRI

2.1.3 Operating Frequencies

The internal resonant frequency of the three converters is 10 kHz. The controller will be designed considering internal resonant frequencies up to 100 kHz.

The input of the 5-kW ac-dc converter is three-phase 60 Hz, sine wave. The controller will be designed considering an input frequency up to 2.5 kHz.

2.1.4 Output Characteristic

The controller will provide a current-limited voltage regulator output characteristic for the SRI power stage. The voltage regulator will operate from 10% of rated load to rated load.

2.1.5 Environmental Requirements

2.1.5.1 Temperature Requirements - The control and protection circuitry shall be designed to work within specification in the temperature range of -40 to 85°C.

2.1.5.2 Radiation Requirements - The control and protection circuitry shall be designed with piece parts that will withstand 10^5 rads (SI). Local shielding will be required to ensure that the electronic piece part dose rate does not exceed 10^5 . Although not required to be built with radiation-hard piece parts, the prototype control and protection circuitry shall be designed with piece parts that have radiation-hard equivalents.

2.2 CONTROL AND PROTECTION ANALYSIS

The objectives of the control and protection analysis were to review the control and protection approaches in each of the three existing APL SRI-based converters, to determine which control and protection functions are necessary (both essential and nonduplicate), and to develop an architecture that can be used with all three existing topologies (half bridge dc-dc, full bridge ac-dc, and dual bridge dc-dc).

The three existing APL SRI were analyzed. Table 2.2-1 summarizes the control and protection tasks.

Table 2.2-1 Summary of Control and Protection Tasks

- | |
|---|
| <ul style="list-style-type: none">o Detection of SCR Reverse Biaso Firing Pulse Generationo Output Voltage and Current Controlo Protection from Catastrophic Failureo Start-Upo Phase Control (Three-Phase ac-dc Unit) |
|---|

The fundamental protection problem arises from the basic topology of all three power stages: half bridge, full bridge, or twin full bridge. In any bridge configuration, two SCRs are in series across the source. If for any reason one SCR is triggered on while the other is conducting, the SCRs may be destroyed by short-circuit current from the source. The fundamental protection function is to ensure that one SCR is off before the other is triggered on. Directly related to this function is accurate sensing of the SCR state. Sensing of the SCR state involves determining whether the anode-to-cathode voltage is forward or reverse-biased. Every SCR has a reverse recovery time (T_Q). After an SCR has been forward-biased and conducting, it must be reverse-biased for a time not less than T_Q before it recovers its ability to block forward voltage. The protection function, then, includes sensing the SCR reverse bias and inhibiting SCR triggering until the T_Q requirement has been met.

A specific control function is associated with generation of the firing pulse to trigger the SCRs on. Specific functions are also associated with controlling the output voltage and current. These include a fast loop for cycle-by-cycle control of the current and a slower loop for voltage control.

Specific functions are also required to start the SRI. The protection circuitry required to ensure two series SCRs are never fired at the same time complicates the task of the start-up circuitry. The start-up function includes using the polarity of the resonant capacitor voltage to determine which SCR to fire first. Because of unbalanced leakage in the SCRs, the initial resonant capacitor voltage can be of either polarity. The initial SCR fired will be chosen so the resonant capacitor voltage adds to the source voltage. In addition, the start-up circuitry overrides the protection circuitry for one cycle to allow the power stage to start. The start-up circuitry also provides a clock signal to initialize the three-phase control unit.

The three-phase control unit requires additional functions to determine when an input phase transition has taken place, to determine when the proper back-bias signals have been received based on the phase pair, and to give SCR fire commands based on the phase pair. The three-phase unit must generate SCR fire commands for two discrete modes: first, when the SCR functions as an SCR, and second, when the SCR functions as a diode.

2.2.1 Previous Approaches

Analysis of the three existing SRI control circuits revealed the following approaches were used to implement control and protection.

It was found that distributed rather than centralized logic was used which resulted in more complicated interfaces between functional circuits. Representative areas in which distributed logic functions were found are:

- 1) The 10-kW dc-dc BBS hold-off circuit;

- 2) The three-phase configuration BBS antisaturation circuit;
- 3) The 200-kW dc-dc configuration firing pulse generator inhibit circuit.

It was found that functions had been duplicated. In the 10 kW dc-dc configuration, there were double-sided start circuits, multiple "FIRE" prevention circuits to inhibit toggle action, and duplicate means of preventing overvoltage.

It was also found that there were multiple circuit designs to perform the same functional task in different topologies. There were also different circuit designs for the firing pulse generator for the 5 kW ac-dc and 200 kW dc-dc configurations.

It was also found that discrete logic had been used rather than integrated circuit logic.

2.2.2 Criteria for Partitioning of Functional Tasks

The object of the partitioning task was to simplify the architecture, produce simple, logical interfaces, remove duplicated functions, and ensure that general-purpose functions are defined that can be used in all configurations (except functions that are unique to the ac-dc unit).

2.2.3 New Architecture and Functional Units

The new architectural approach is based on:

- 1) Centralized logic;
- 2) Functions identified as necessary and nonduplicate;
- 3) Circuits capable of performing their functions in all topologies;
- 4) Use of IC technology.

Using the partitioning criteria, the control and protection tasks have been grouped into the five functional circuits:

- 1) Back-bias sensor;
- 2) Firing pulse generator;
- 3) Protection unit (includes start-up function);
- 4) Three-phase unit;
- 5) Control unit.

2.2.4 Results of Existing SRI-Based Converter Evaluations

Table 2.2-2 summarizes the results of the 10-kW converter evaluation. Two items in the converter design were found that had not been

pointed out in the open literature. First was an inversion in the controller integrator and second was the use of the resonant capacitor voltage as an input to the protection circuit. These discoveries aided in a detailed understanding of the 10-kW unit operation that could be extended directly to the 5-kW and 200-kW units.

Table 2.2-2 Results of 10-kW Converter Evaluation

Observation	Significance
Inversion in Controller Integrator	This inversion not shown in open literature; addition to practical knowledge.
Use of Resonant Capacitor Voltage Protection Circuit	Never shown in open literature; additional knowledge.
Detailed Understanding of 10 kW Unit	Understanding directly applicable to 5-kW and 200-kW units.

Table 2.2-3 summarizes the results of the evaluation of the 5-kW ac-dc and 200 kW dc-dc units.

Table 2.2-3 Results of 5-kW and 200-kW Evaluations

<u>5 kW ac-dc</u>	
-	Established unique Requirements for 3-Phase Back-Bias Sensor
-	Prepared Electrical Drawings for Selected Cards
-	Developed Selected Back Plane Wiring Information
<u>200 kW dc-dc</u>	
-	Determined that controller Uses an Apparent Nonresetting Integrator
-	Developed Electrical Schematics for All Cards

2.3 IC TECHNOLOGY STUDY

The purpose of this study was to identify IC process and fabrication technologies for the control and protection circuits. Although the goal was to identify technologies that were compatible with wide use and high production rates, only prototype quantities will be produced for this contract.

Another general study guideline was to consider the possibility and difficulty of radiation-hardening the chosen process technology. Although there was no requirement for the prototypes to be radiation hard, the ability to implement the prototype designs in a radiation-hard technology was considered.

The IC technology study consisted of a survey of process technology (bipolar or MOS), a survey of fabrication technology (custom ICs, commercially available ICs, gate arrays, and hybrids), a discussion of the options for each functional circuit, and recommendations for the process and fabrication technology for each of the functional circuits.

2.3.1 Process Technology - Digital

For digital circuits, the IC process technology can be divided into two categories, bipolar and MOS, with the subdivisions as in Table 2.3-1.

The most common bipolar processes are Transistor-Transistor Logic (TTL), including TTL-LS (low-power Schottky), and ECL. Emitter Coupled Logic (ECL) is a superfast technology and has excellent radiation resistance. On the negative side it consumes high power, requires multiple bias voltages, and has limited family availability. Its very high speed also requires special care in layout and interconnection design. A prominent use for ECL has been in such large mainframe computers as the CRAY series of supercomputers. The AIT series resonant inverters operating up to 100 kHz will not require the speed that ECL provides, such as toggle frequencies in the hundreds of MHz region. ECL is not considered a candidate for AIT. TTL has been the leader in small and medium-scale integration (SSI and MSI) although in recent years it has fallen behind in the trend toward large-scale integration (LSI) because of thermal limitations in high-density microcircuits. TTL-LS represents an improvement in bipolar technology to make it more competitive with the MOS technologies. It has much lower power dissipation than TTL while maintaining relatively good speed and radiation resistance.

Table 2.3-1 Comparison of Integrated Circuit Processes

Integrated Circuit Process	Power Consumption	Speed	Family Availability	Radiation Hardness
Bipolar				
- TTL	Poor	Very Good	Excellent	Very Good
- TTL-LS	Good	Good	Good	Good
- ECL	Very Poor	Excellent	Poor	Excellent
- 1^2	Programmable	Programmable	Poor	Good
MOS				
- NMOS	Poor	Excellent	Poor	
- PMOS	Good	Poor	Good	
- CMOS	Very Good	Good		
- CMOS/SOS	Very Good	Good	Poor	Very Good
- CMOS/BULK	Very Good	Poor	Poor	Very Good

The TTL processes yield 5-V parts. The noise margin for 5-V TTL is approximately 0.4 V or 8% of VCC. Conservative design practice prefers noise margins larger than the 0.4 V available from 5-V TTL.

I²L is still expensive and lacks sufficient industry interest (sources of supply) to be considered a strong candidate for the AIT program. Another criticism that has been leveled at I²L is a lack of standardization as there are large variations from manufacturer to manufacturer.

The generic MOS processes are NMOS, PMOS, and CMOS. NMOS is currently the most popular MOS process although it has a narrow range of operating temperatures, poor radiation resistance, and requires high power. Many sources of supply and a great variety of device types have combined to force its cost to the lowest levels. NMOS is used in many of the microprocessors for such personal computers as the 6502 microprocessor in the Apple 2 Plus.

PMOS has lower power dissipation and better radiation resistance than NMOS but few sources of supply and limited device selection. Its development has been stifled by the development of CMOS.

CMOS represents a near-perfect process technology in many ways. Its quiescent power dissipation is near zero, and its dynamic dissipation increases primarily because of parasitic capacitance loading. Noise immunity is very high (30 percent of supply voltage for both high and low states) and switching noise generation very low relative to TTL and ECL. A particular advantage of CMOS for the AIT program is that it can combine both analog and digital functions. Digitally controlled analog transmission gates are available that can operate with input and output voltages between zero and a full power supply voltage level. These gates are highly useful in systems where analog multiplexing and A-to-D conversion functions are required.

An advantage of CMOS is that it is available in a variety of operating voltages, up to 15 V. By going to 15-V CMOS, a noise immunity of up to 5 V can be obtained. This is 12.5 times the noise immunity of 5-V TTL.

Any process technology selected for AIT should be compatible with space application. This means radiation resistance. The Space Division has established near-term goals for microelectronics radiation tolerance for five-year missions of 5×10^4 rad (Si) minimum in general and 1×10^5 rad (Si) for enhanced survivability missions. The long-term goal is 1×10^6 rad (Si). Unhardened CMOS is good to about 10^4 rad (Si). To overcome this limitation, serious development activities are underway in two areas--CMOS/SOS and CMOS/Bulk. Referring to the substrate, SOS indicates silicon-on-sapphire and Bulk indicates silicon substrate base material. The physics of the Bulk technology are well understood and its capabilities and producibility have been demonstrated by the CRM. Although material problems have plagued CMOS/SOS, it continues to receive heavy emphasis.

Sandia's Bulk technology process has been used to fabricate radiation-tolerant parts since the middle 1970s, first with a metal gate process and subsequently with self-aligned polysilicon gates. They have consistently demonstrated total dose tolerance in the 10^5 rad (Si) to 10^6 rad (Si) range. They have also demonstrated upset levels greater than 10^8 rad/S. They have fabricated tens of thousands of these

hardened parts that have also functioned over the full range of normally specified environments. Many of the parts were subjected to full Class S screening and quality assurance procedures.

Appendix A gives further information about radiation-hard micro-processor chip sets.

2.3.2 Process Technology - Linear

The basic process technology for linear ICs is bipolar monolithic. Two sources were used to gather information about radiation-hard linear ICs--first the CRM at Sandia National Laboratories, and second, the Parts Technology group at Martin Marietta Denver Aerospace.

At the time of this survey, CRM did not have any radiation-hard linear circuits in production (operational amplifiers or comparators). CRM anticipates some operational amplifiers in production within two years, but they have no comparators scheduled (Ref 4). Therefore CRM is not a source of radiation-hard linear circuits for the prototype phase of the AIT program.

The Parts Technology group at Martin Marietta is responsible for selecting parts for the radiation-hard circuits to be produced in the near term. They have surveyed commercial manufacturers and compiled a list of linear IC, digital IC, transistor, and passive component producers who have published data demonstrating radiation hardness. It was concluded that fabrication of radiation-hard electronics using commercially available components in the near term will require the following guidelines. Electronic piece parts that can be produced in the near term are considered acceptable for use with appropriate derating at 10^5 rad (SI) total dose. If the background dose is higher than this level, local shielding should be used to reduce the total dose at the piece part of 10^5 rad (SI).

Table 2.3-2 summarizes linear piece parts demonstrating acceptable radiation hardness to 10^5 rad (SI).

Table 2.3-2 Linear ICs with Demonstrated Radiation Hardness to 10^5 rad (SI)

Generic P/N	Manufacturer	MIL-M-38510	Description	Hardness Status
LM101A	NSC	10103	Op amp	Acceptable
LM103	NSC	None	Ref Diode	Acceptable
LM105	AMD	None	Adj Volt Reg	Acceptable
LM108A	AMD	10104	Op Amp	Acceptable
LM111A	AMD	10304	Comparator	Acceptable
LM113	NSC	None	Ref Diode	Acceptable
LM124	AMD	11005	Quad Op Amp	Acceptable

Discrete bipolar transistors are subject to beta degradation and saturation caused by ionizing radiation. The radiation can cause an increase in photocurrents that appear as an increase in collector-to-base leakage, causing the transistor to saturate. Low-frequency bipolar transistors are more radiation-sensitive than high-frequency transistors. Therefore, a suggested radiation hardening guideline is to choose transistors with as high a cutoff frequency as possible.

2.3.3 SCR Radiation Discussion

An SCR is a four-layer bistable switch that depends on a p-n-p-n structure for regenerative feedback. When the SCR loop gain is less than 1, it is off. When its loop gain is made greater than 1, it is switched on. It is normally turned on by injecting current into the gate. The photocurrents caused by ionizing radiation can produce an apparent gate current increase. If the photocurrents induce gate current exceeding the turn-on threshold, the SCR will be turned on by radiation. A general rule is that the dose rate required to turn a SCR on is proportional to the gate current required to turn on the SCR. The higher the gate current required to turn on the SCR, the higher the dose rate threshold for turn-on. At the present time, radiation-tolerant flight-type SCRs have not been identified.

2.3.4 Fabrication Technology

Table 2.3-3 summarizes the candidate fabrication technologies. The most desirable technology for the control and protection circuits is custom IC. Custom IC will yield the lowest unit cost per circuit and will hasten the wide acceptance and use of the SRI. The fabrication technology characteristics show that they differ in initial cost, development time, time to produce the first prototype, and lot size for economic production. Custom ICs have the highest initial cost, longest development time and the highest lot size for economic production, but the lowest unit cost. Custom ICs may require from \$0.1M to \$1.0M for initial cost and require up to a year for delivery of prototypes.

Table 2.3-3 Candidate Fabrication Technologies Compared

Candidate	Initial Cost	Development Time	Reliability	3-Phase Controller	All Other Control Circuits
Custom IC	Highest	Highest	Highest	Yes	Yes
Gate Array	Lower	Lower	High	Yes	No
Hybrid	Lower	Lower	Lower Than Gate Array	Yes	Yes
Discrete	Lowest	Lowest	High	Yes	Yes

A candidate technology for the three-phase controller is a gate array because the three-phase controller is primarily digital. Gate arrays are not a candidate for any other AIT control circuit. Commercial gate arrays from silicon foundries have been estimated to have an 8- to 12-week turnaround time (from design input to delivery of prototype chips) with a cost of \$10k to \$30k.

The fabrication technology compatible with the low-production scenario for the prototypes in this contract is hybrid circuits. Hybrid circuit technology is a candidate fabrication technology for all control and protection circuits.

A hybrid circuit fabrication of the three-phase controller is compatible with radiation hardening. The prototype will be built with commercial 4000-series CMOS chips that are not radiation-hard but do have radiation-hard equivalents to 10^6 rad (SI). The three-phase controller can be made radiation-hard by substituting the radiation-hard chips from RCA for the commercial 4000-series chips. The linear ICs from Table 2.3-2 that have radiation-hard equivalents will be used for prototype fabrication.

2.3.5 Options

Table 2.3-4 summarizes the options for the three-phase unit. There are no theoretical problems with implementing the three-phase controller by a commercial CMOS gate array. The controller will require approximately 100 gates, which is pedestrian. Mask-programmable gate arrays are capable of speeds up to 10 MHz. A maximum frequency of 2.5 kHz for the three-phase unit and a maximum of 0.1 MHz for the resonant frequency is required. The most practical option for the three-phase unit is considered to be hybrid circuit technology because of the availability of radiation hard 4000-series CMOS.

Table 2.3-4 Three-Phase Controller Options

Option	Can Design Be Built with Radiation-Hard Parts?	Comment
1) Use Gate Array from Conklin Chip Set	Yes	Not practical; hardened gate array not in production at Sandia.
2) Commercial CMOS Gate Array from a Silicon Foundry	Qualified Yes	By using CRM radiation-hard design constraints and only cells available from CRM Library, there would be minimum effort to fabricate in GUA array at CRM.

Table 2.3-4 (concl)

Option	Can Design Be Built with Radiation-Hard Parts?	Comment
3) Hybrid Circuit	Yes	Prototype with 4000-series CMOS; substitute radiation-hard 4000-series CMOS for later builds; no additional design required for radiation hardening.

Table 2.3-5 summarizes the options for the FPG, BBS, control unit, and protection unit. Commercial linear arrays are not considered strong candidates because of the lack of radiation-hardened versions of the linear arrays. There are only digital gate arrays, no linear arrays, in the Conklin chip set that is being radiation hardened by CRM. Hybrid circuits are the most practical option for the prototype fabrication.

Table 2.3-5 Options for FPG, BBS, Control Unit, and Protection Unit

Option	Can Design Be Built with Radiation-Hard Parts?	Comment
1) Commercial Linear Array	No	Theoretically a possibility, but the number of linear arrays is very small compared to digital gate arrays.
2) Hybrids	Yes	Hybrid fabrication most practical for the prototype production quantities envisioned; suggest design be done using LM108 and LM111 parts that have radiation-hardened equivalents.

2.3.6 Recommendations

The recommendations for the fabrication and IC technologies for the circuits are summarized in Table 2.3-6. Hybrid circuits are recommended for the firing pulse generator, back-bias sensor, protection unit, and the three-phase unit. Discrete ICs are recommended for the control unit because the many external components required to customize the control circuit to the particular SRI negate any advantage in hybridizing the control circuit at this time. For digital circuits, RCA 4000-series commercial CMOS is recommended for the prototypes. Radiation-hard equivalents of the 4000-series CMOS can be used for later builds to produce radiation-hard circuits. We recommend the

prototypes be built with commercial equivalents of the demonstrated radiation-hard linear circuits from Table 2.3-2.

Table 2.3-6 IC Technology and Fabrication Recommendations

Unit	Fabrication Technology	IC Technology
Three-Phase	Hybrid	RCA 4000-series CMOS for prototype; substitute radiation-hardened RCA 4000-series for flight.
FPG, BBS, Protection	Hybrid	Monolithic bipolar, LM108 and LM111 for linear, digital same as three-phase.
Control	Discrete	Monolithic bipolar, LM108 and LM111.

2.4 FUNCTIONAL DESIGN

2.4.1 Objectives

The objectives of the functional design task were to:

- 1) Identify the functional elements;
- 2) Generate system block diagrams for each of the three existing APL SRI topologies;
- 3) Generate functional requirements for each functional block;
- 4) Perform a functional design for each functional block to the block diagram and schematic level.

This section describes the system-level block diagrams. Conceptual design of the functional blocks will be discussed in Section 2.5 (custom part specifications).

2.4.2 Partitioning

The control and protection functions were partitioned into the following five areas:

- 1) Back-bias sensor;
- 2) Firing pulse generator;
- 3) Protection unit;
- 4) Three-phase unit;
- 5) Control unit;

2.4.3 10-kW dc/dc Block Diagram

Figure 2.4-1 is a conceptual block diagram of the proposed control and protection circuit configuration for the 10-kW dc-dc converter.

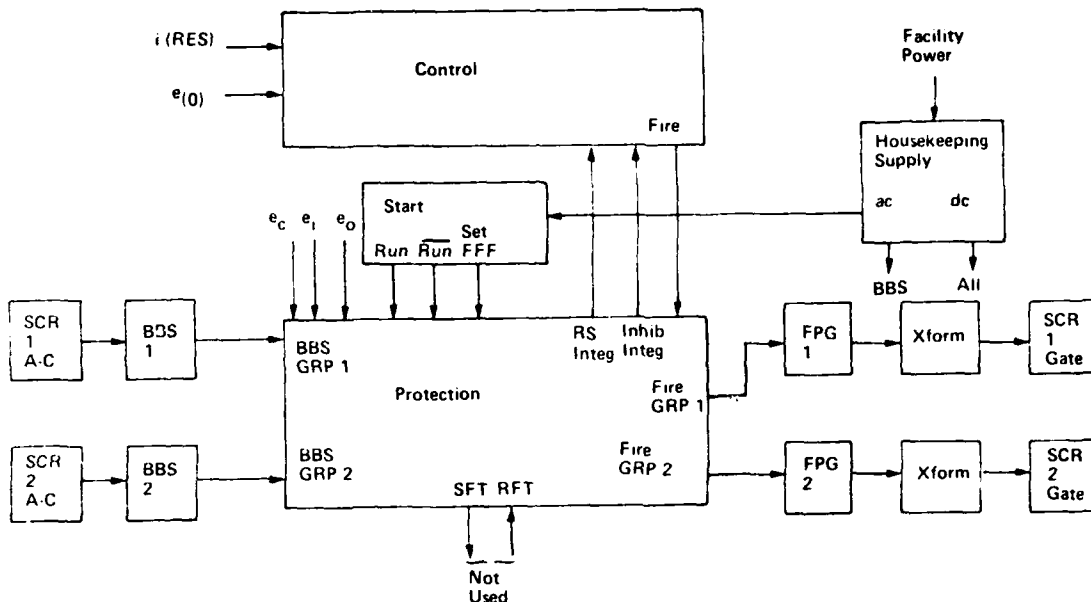


Figure 2.4-1 10-kW dc-dc Simplified Functional Block Diagram

The significant features of the 10-kW dc-dc power stage are that it is a half bridge with two SCRs, two BBSs, and two FPGs. There is one control unit, one protection unit, and one housekeeping power supply. The start function is shown as a separate block to highlight it, but it will functionally be incorporated in the protection unit. The housekeeping supply includes a debounce circuit for the logic start signal. All signals for the different functional blocks are identified in the figure. Safe for transition (SFT) and request for transition (RFT) are handshake signals for the three-phase configuration that are not used in the dc-dc configurations. The feedback parameters used for control are the resonant current and the output voltage.

2.4.4 5-kW ac-dc Block Diagram

Figure 2.4-2 is a block diagram of the control and protection circuit configuration for the 5 kW ac-dc converter. The significant features of the 5-kW ac-dc configuration are that each of the 12 SCRs functions as an SCR 1/3 of the time, a diode 1/3 of the time, and is inactive 1/3 of the time. There are six phase pairs within 360 electrical degrees. The phase pairs must be sensed, and while the system is operating within a phase pair, the system equivalent circuit is that of a full-bridge SRI-based converter.

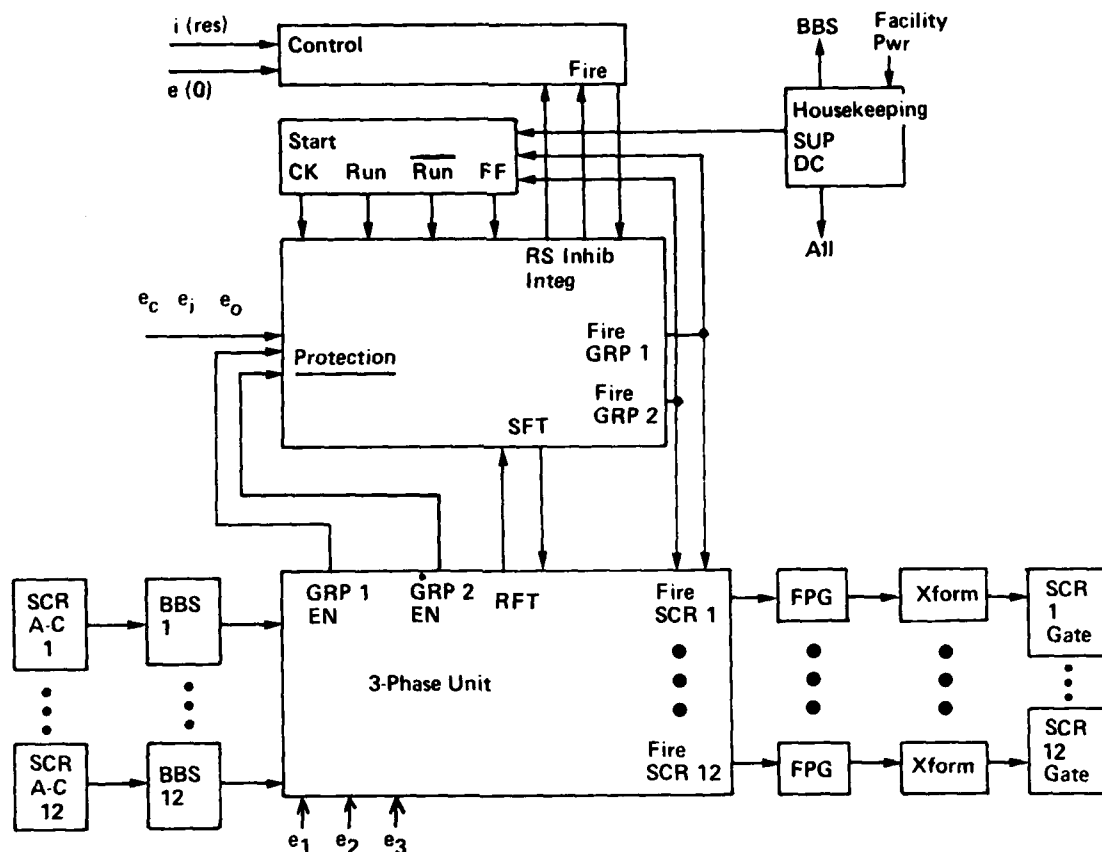


Figure 2.4-2 5-kW Three-Phase ac-dc Simplified Functional Block Diagram

The control and protection circuit includes 12 BBSs and 12 FPGs, one for each of the 12 SCRs. The three neutral to phase voltages are inputs to the three-phase unit where they are used to determine the instantaneous operational phase pair. The RFT signal is generated in the three-phase unit and sent to the protection unit. When the protection unit determines it is safe to go from one phase pair to another, it responds by sending a SFT signal to the three-phase unit. The feedback parameters used for control are the resonant current and output voltage.

2.4.5 200 kW dc/dc Block Diagram

Figure 2.4-3 is a block diagram of the control and protection circuit configuration for the 200-kW dc-dc converter. The significant features of the power stage topology are that there are twin full bridges, eight SCRs, and each SCR is provided with an antiparallel diode. The SCRs function as SCKs only. They do not have to function as diodes as in the three-phase configuration. Each SCR is used, at most, 50% of the time.

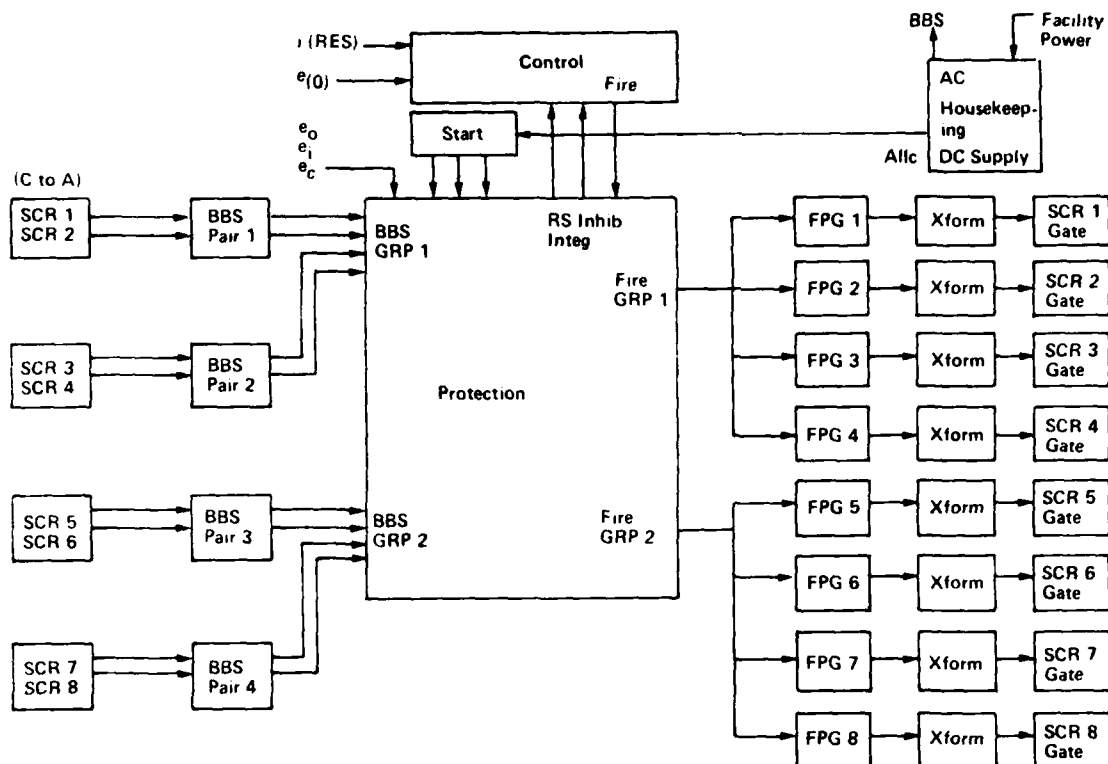


Figure 2.4-3 200-kW dc-dc Simplified Functional Block Diagram

Significant features of the control and protection circuit are the eight BBSs and eight FPGs. Because there are two full bridges for one direction of resonant current two SCRs must be fired for each bridge, or a total of four for the two bridges. The four SCRs associated with the same direction of resonant current are fired from the same protection unit signal. The firing pulse generators are all referenced to signal ground. The SCR gate and cathode circuit are isolated from signal ground with a transformer. The resonant current and the output voltage are the feedback variables for control.

2.5 CUSTOM PART SPECIFICATIONS

There will be five custom parts: (a) firing pulse generator (b) back-bias sensor (c) protection unit (d) three-phase unit and (e) control unit. The detail requirements are described in the following subsections.

2.5.1 Firing Pulse Generator

2.5.1.1 Background - The three SRI power stages all use SCRs as the power-switching device. The fundamental interface requirements for an

SCR gate circuit are the open-circuit voltage, the equivalent series resistance, and the pulse width. A survey of modern large SCRs revealed that they all have approximately the same gate turn-on requirements. The modern SCRs all have amplifying gates. The gate current at turn-on is specified as 150 mA and the voltage as 3 V. Turn-on times are typically 3.5 microseconds maximum. Figure 2.5.1-1 shows typical SCR turn-on delay time as a function of gate current. The figure shows that a gate current of 0.5 amp produces a delay time of 1 microsecond. Gate currents larger than 0.5 amp provide only marginal reductions in the delay time. The rise time of the current should be less than one microsecond.

Another factor that influences the required open-circuit voltage for the SCR gate drive circuit is the time rate of change of current (di/dt) that must be supported while the SCR is turning on. If the maximum specified di/dt is called for, an open-circuit voltage of up to 15 V can be required (Ref 5). From an analysis of existing SRI converters it is apparent that they have been designed for a low di/dt during SCR turn-on. For example, the 200-kW dc-dc unit has a maximum di/dt of 6 amps per microsecond. This is much less than the 100-amp per microsecond the SCR is rated for. When the circuit of the 200-kW FPG was analyzed, we found that the open-circuit voltage was 6 V. In the 200-kW FPG, there was no intentional series resistance. Only the parasitic resistance in the circuit was used to limit the gate current.

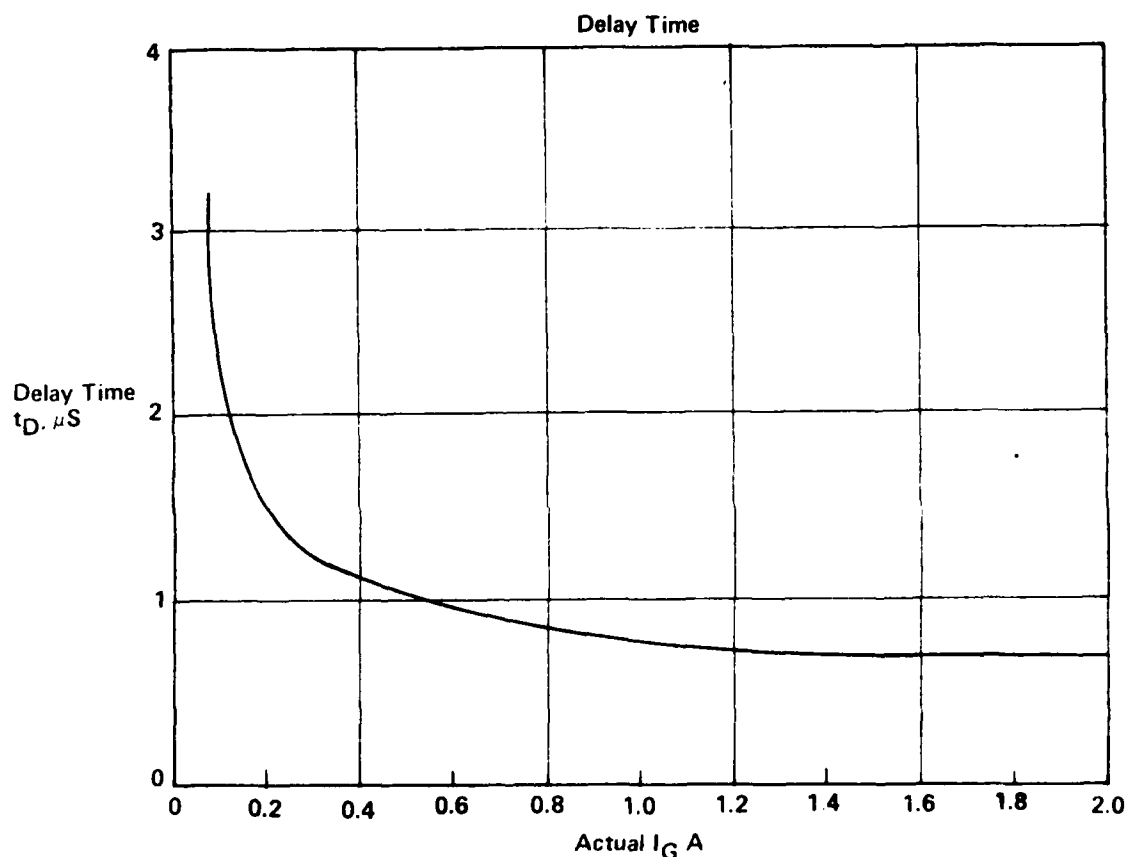


Figure 2.5.1-1 Typical SCR Turn-On Characteristics

Figure 2.5.1-2 shows an idealized representation of the FPG current waveform. There are six adjustable parameters: four current levels (I_{P1} , I_{P2} , I_{DC1} and I_{DC2}), and two pulsewidths (T_{P1} and T_{P2}).

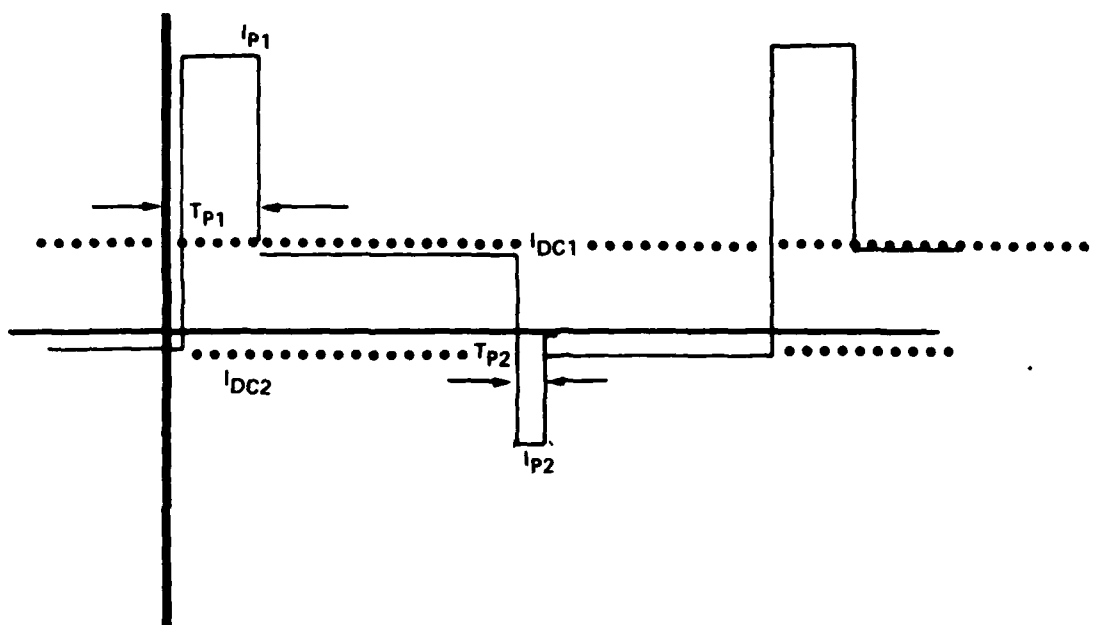


Figure 2.5.1-2 FPG Current Waveforms

A discussion of the FPG characteristics for the power switch drive combinations shown in Figure 2.5.1-3 follows. The SCR direct drive requires a current pulse from the FPG for SCR turn-on but no sustaining current to hold the SCR on. A gate-assisted turn-off (GTO) SCR will require a current pulse for minimum turnoff time. For driving a bipolar transistor with proportional drive, the FPG must supply both turn-on and turn-off pulses. The proportional feedback will supply the base current to hold the bipolar transistor on. Because bipolar direct drive requires the FPG to supply all of the base current while the transistor is conducting, it is not practical for large SRI-based converters.

A MOSFET requires only gate voltage for continuous conduction. The FPG must supply an initial turn-on current pulse to charge the gate capacitance and a sustaining current to maintain voltage on the gate clamp. For turn-off the FPG must supply a negative current pulse to discharge the gate capacitance and a sustaining current to maintain the reverse voltage clamp.

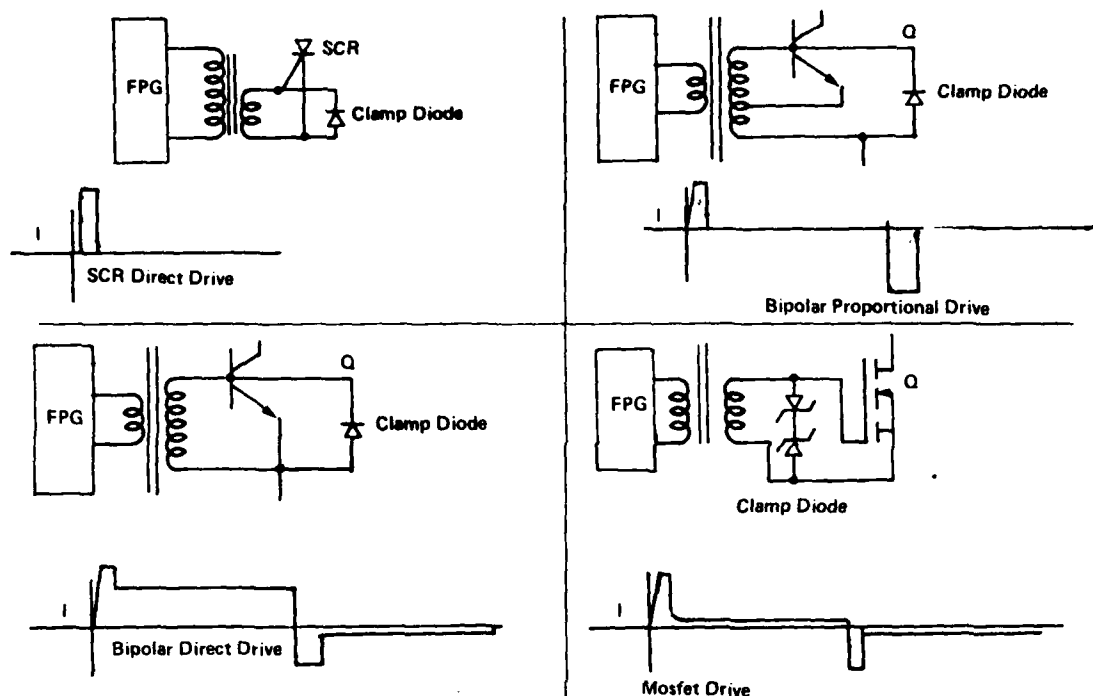


Figure 2.5.1-3 Possible Drive Combinations

An investigation was made to determine the compatibility of requirements for the SCR drive and bipolar transistor drive. From tests of the 5-kW ac-dc and 10-kW dc-dc breadboards, it was found that actual firing pulse generator requirements could be met by an open-circuit voltage of 9 V, a peak current of 1.5 amps, and a pulsewidth of 4 microseconds. In Ref 6, Robson and Hancock described the development of base drives for SRI using the bipolar transistors D60T and D70T. In their paper, they list the following as turn-on pulse requirements for proportional drive.

<u>Transistors</u>	<u>Pulse Amplitude, A</u>	<u>Pulse Width, ms</u>
D60T	12	15
D70T	30	10

From these considerations, it does not appear a single firing pulse generator will be optimum for both an SCR and a bipolar proportional drive. A circuit that is designed for a 1.5-amp SCR pulse will be too small for the bipolar drive. If the firing pulse generator is designed to supply either 12- or 30-amp pulses for bipolar drive, the circuit will be greatly oversized if used with an SCR. During the detailed design phase, attempts will be made to reconcile the conflicting requirements of an SCR and bipolar transistor proportional drive for a single drive circuit.

2.5.1.2 Requirements - As a minimum, the firing pulse generator must function with the three existing SCR power stages. The firing pulse generator must have the following characteristics:

- 1) Open-circuit voltage - 15 V;
- 2) Peak current - 2 amps;
- 3) Pulsewidth - To 10 microseconds where these parameters can be made smaller by changing circuit components.

This set of requirements will allow the same SCR gate firing circuit to meet the requirements for the three existing APL converters and also provide lower gate voltages and currents for minimum gate circuit dissipation and maximum efficiency.

2.5.1.3 Block Diagram - Figure 2.5.1-4 is a block diagram of the SCR FPG with transformer isolation. The transformer provides isolation between signal ground and the SCR gate and cathode.

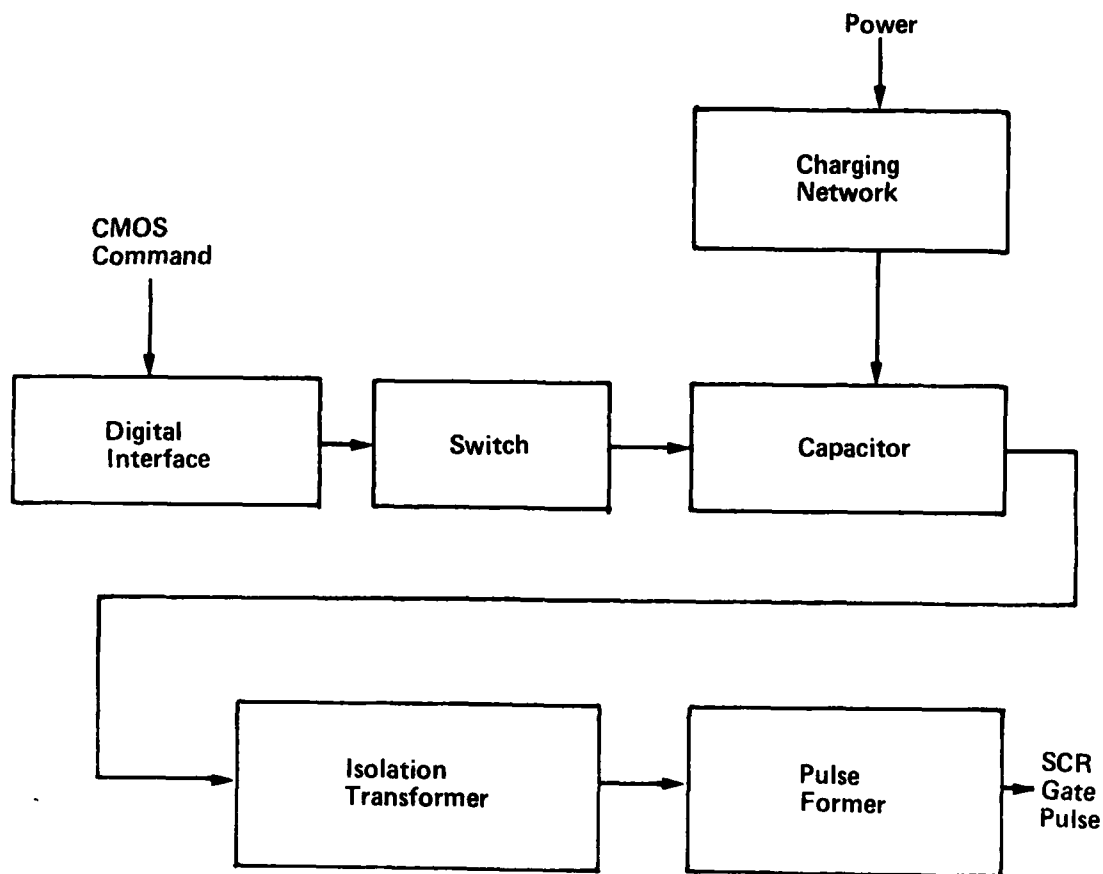


Figure 2.5.1-4 FPG Block Diagram

2.5.1.4 Circuit Diagram - Figure 2.5.1-5 shows a circuit diagram for the capacitor discharge FPG. The components inside the dashed lines are those to be incorporated in a hybrid circuit. The switch is composed of Q1, Q2, and Q3. Energy storage capacitor C1 is charged through R2, and T1 is the isolation transformer. The pulse characteristics can be controlled by varying C1, the turns ratio of T1, or by varying R3.

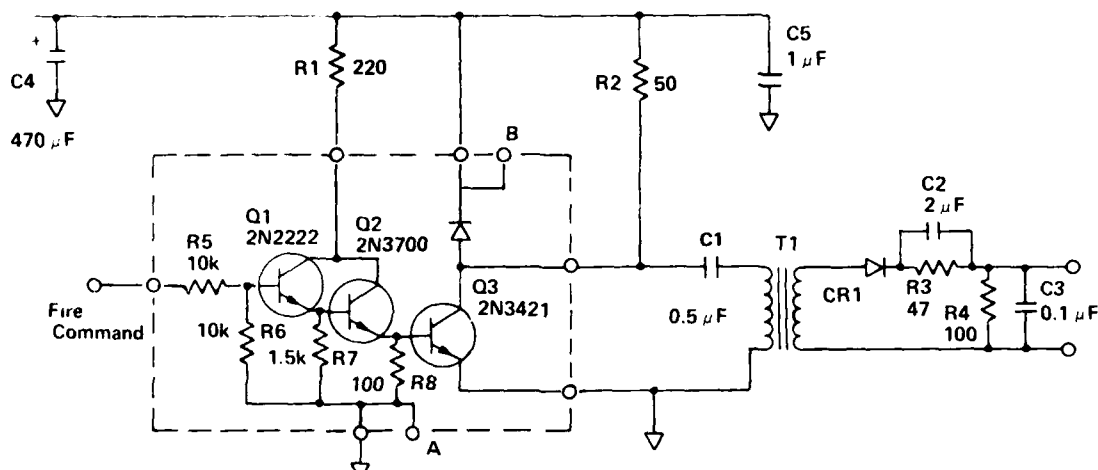


Figure 2.5.1-5 FPG Schematic

2.5.1.5 Power - The FPG shall be provided with 15 V, $\pm 10\%$. The fire command to the FPG shall be a positive true signal from the 15-V CMOS.

2.5.1.6 Parts List - The parts list is summarized in Table 2.5.1-1.

Table 2.5.1-1 FPG Parts List

Reference Designator	Description	PN
Q3	NPN Transistor	2N3421
Q2	NPN Transistor	2N3700
Q1	NPN Transistor	2N2222
T1	Core	846T250-3C8

2.5.2 Back-Bias Sensor

2.5.2.1 Background - In all of the topologies for the three SRI-based inverters, there is an SCR with an antiparallel diode to provide soft commutation of the SCR. There is only one diode drop of reverse voltage across the SCR when the SCR is to turn off. The fundamental BBS problem is to sense one diode drop in the 600-V common mode and have the BBS survive the 600-V common mode.

A characteristic of all SCRs is that after the SCR is forward-biased, it must remain reverse-biased for a time equal to the reverse recovery time (T_Q) before it can block forward voltage. Therefore to ensure the SCR will be recovered and able to block forward voltage, it is necessary to sense when the SCR is reverse-biased, then wait T_Q seconds before triggering the opposing SCR that would forward-bias the off SCR. The BBS sensor will sense SCR back-bias. The delay to assure SCR recovery will be provided in the protection unit.

2.5.2.2 Requirements - Table 2.5.2-1 summarizes the derived requirements for the back-bias sensor. A single design will be capable of sensing either positive or negative voltage with respect to BBS common. The BBS may be packaged in pairs, but the two returns must be separate. Each BBS will have an isolated power supply. The BBS must be able to sense one diode drop reverse voltage on one-half cycle and not be damaged by up to 600-V forward voltage on the next half-cycle.

Table 2.5.2-1 Back-Bias Sensor Requirements

-	Back-Bias Voltage, -0.2 to -0.4 V
-	Differential Mode Voltage of 600 V Square Wave across the Inputs
-	Output Compatible with CMOS Logic Family
-	Maximum Signal Delay to be Kept under 1 microsecond
-	A Single Design Capable of Sensing Positive or Negative Reverse Bias Voltage with Respect to BBS Common
-	Isolated Power Supply

The logic output of the BBS as a function of the SCR anode-to-cathode voltage is tabulated.

<u>SCR Anode to Cathode Voltage</u>	<u>Logic Output of BBS</u>
+ (Forward-Biased)	0
- (Reverse-Biased)	1

2.5.2.3 Block Diagram - Figure 2.5.2-1 shows a block diagram of the dual BBS. The significant features are that the two comparators and their associated components will be in a hybrid; a square wave oscillator and transformer will be used to supply isolated power to the two comparators, an optocoupler will be used for signal isolation, and a level translator circuit will interface the 5-V optocoupler with the 15-V CMOS. The isolation transformer, optoisolator, and level translator will be external to the hybrid. The optoisolator is not compatible with hybrid design because it must withstand 600 V and hybrid packages are only normally good for 50 V from pin to pin. Also of significance is that the returns of the two BBSs will be fully isolated because in the 200-kW unit SCRs that have anodes electrically connected have separate anode sense leads brought out for the BBS.

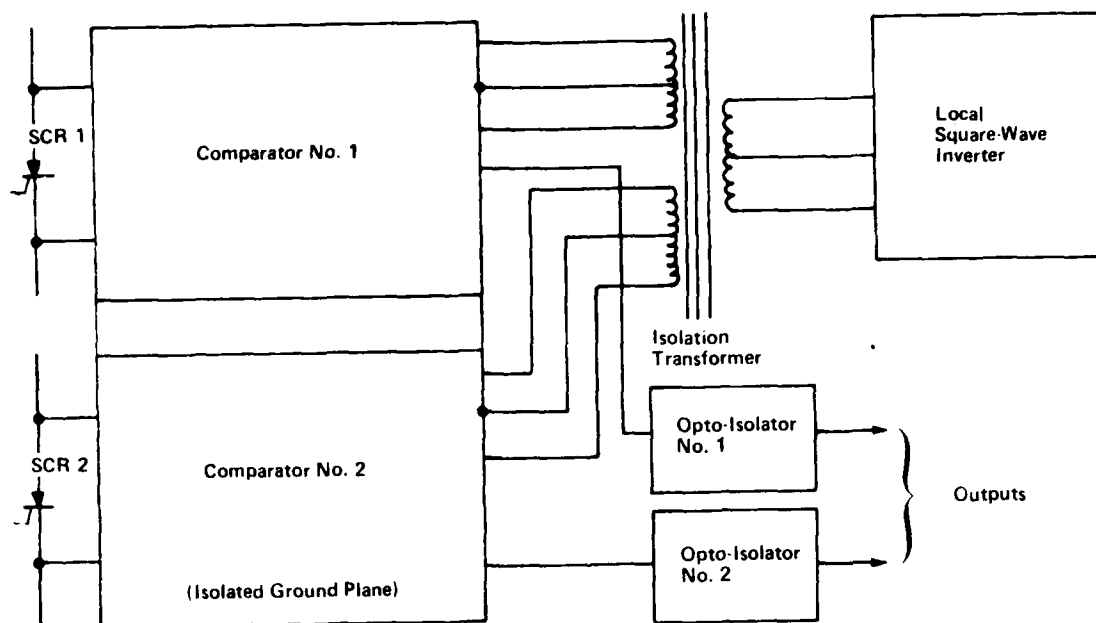


Figure 2.5.2-1 BBS Block Diagram

2.5.2.4 Circuit Schematic - Figure 2.5.2-2 shows a conceptual circuit schematic of the back-bias sensor comparator. R1 will be external to the hybrid because it will have 600 V across it and dissipate up to 1 W. R1, along with CR1 and CR2, protect the comparator inputs from 600 V. To sense either a positive or negative voltage with respect to return, point A as well as the inverting and noninverting comparator inputs must be brought out of the circuit for external connection. For a negative sensor, point A is connected to the noninverting input.

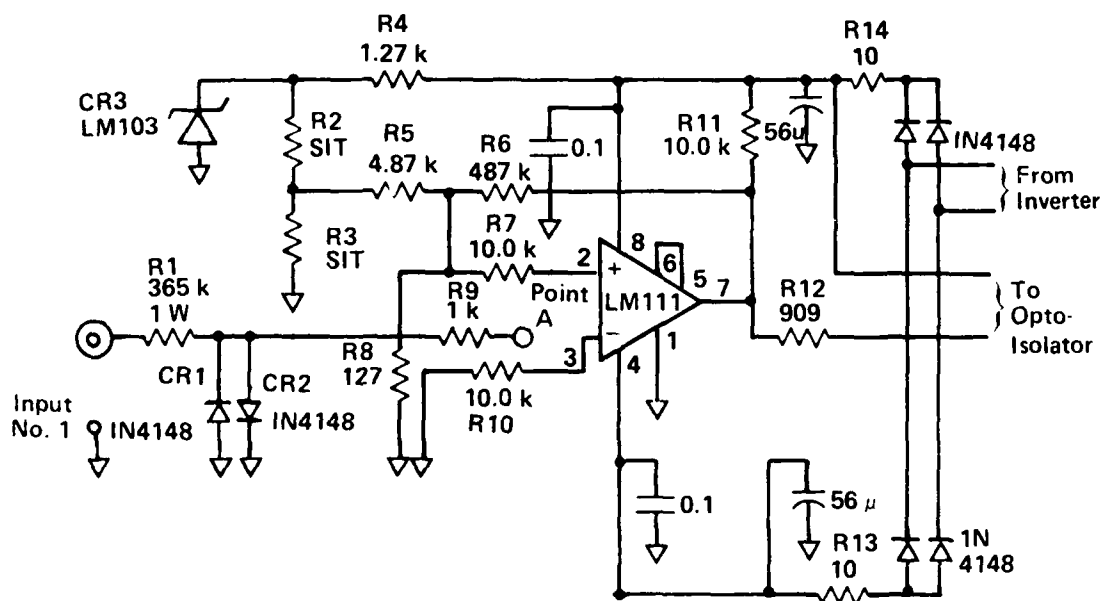


Figure 2.5.2-2 BBS Schematic of One Comparator

For a positive sensor, point A is connected to the inverting input. A stable voltage reference is provided by voltage divider R2 and R3 and the regulator diode CR3. Positive feedback and hysteresis is provided by R6 and R8. R12 is used to limit the current to the photodiode.

2.5.2.5 Power - The BBS will be supplied with transformer-isolated ac power. The ac power source shall be square wave, 20 kHz $\pm 10\%$, and 15 V $\pm 10\%$ peak-to-peak.

2.5.2.6 Parts List - Table 2.5.2-2 summarizes the BBS parts.

Table 2.5.2-2 BBS Parts List

Description	PN
Comparator	LM111
Optoisolator	6N134
Transformer Core	2616C-A1000-3B7

2.5.3 Protection Unit

2.5.3.1 Background - All of the SRI topologies require two series switches to be placed across the source. Should these switches be turned on at the same time, they would be destroyed. One of the primary requirements for the protection unit is to prevent simultaneous conduction of these SCRs. The power switches are divided into two groups that are alternatively toggled during inverter operation. The protection unit must provide this toggle function between groups of power switches. It includes limit checking and control integrator inhibit for the resonant capacitor voltages, source voltage, and output voltage.

The protection unit must work with both a dc-dc and ac-dc converter. To add the ac-dc compatibility to the dc-dc protection unit, two additional handshake signals are required. An RFT signal will be generated in the three-phase unit. The protection unit will respond to this by ensuring that all SCRs are off, all SCRs that were used as diodes have stopped conducting, and the resonant current has decayed to zero. Then, the protection unit will issue a SFT to the three-phase unit and the SRI will be restarted.

The initial start function is also included in the protection unit. When in the off state but with control power applied, the initial conditions of all flip-flops are controlled. When power is applied to the power stage, the polarity of the resonant capacitor will vary depending on switch leakage. The polarity of the resonant capacitor voltage will be used to select the initial set of SCRs to be turned on. The set of

SCRs will be selected so the resonant capacitor voltage adds to the source voltage. This is done to ensure maximum resonant current on the initial pulse. When the start signal is received, the protection unit will issue a SFT to the three-phase unit, delay, and then clock a fire command. After this one initial fire pulse, the normal operation commences.

2.5.3.2 Requirements - Table 2.5.3-1 gives the top-level functional requirements for the protection unit.

Table 2.5.3-1 Protection Circuit Top-Level Requirements

- After Group 1 SCRs are fired, a back bias signal from Group 1 shall exist for t seconds before Group 2 shall be enabled to fire.
- The SCRs shall be divided into two groups and shall be fired alternately.
- RFT (Request for Transition) - When this signal from the three-phase controller is true, it shall inhibit SCR fire commands.
- SFT (Safe for Transition) - This is generated in the protection unit in response to an RFT from the three-phase controller. Once RFT is true and there are no SCR fire commands, the protection unit shall look for a 1-0 transition on the back-bias sensors, delay t seconds, and send a SFT high true to the three-phase controller.
- Resonant capacitor or input voltage out of limits shall inhibit the Fire Group 1 and 2 SCR signals.
- The output voltage out of limit shall inhibit the integrator in the control circuit.
- When not connected, there shall be a minimum of 1 megohm at 2 V common mode between input and signal return and 1 megohm at 2 V common mode between output and signal return at dc.

As shown in the block diagram of Figure 2.5.3-1, the protection unit is partitioned into three functional areas: (1) SCR fire generator and digital protection (2) start circuit and (3) analog protection.

The functional requirements for each area are described.

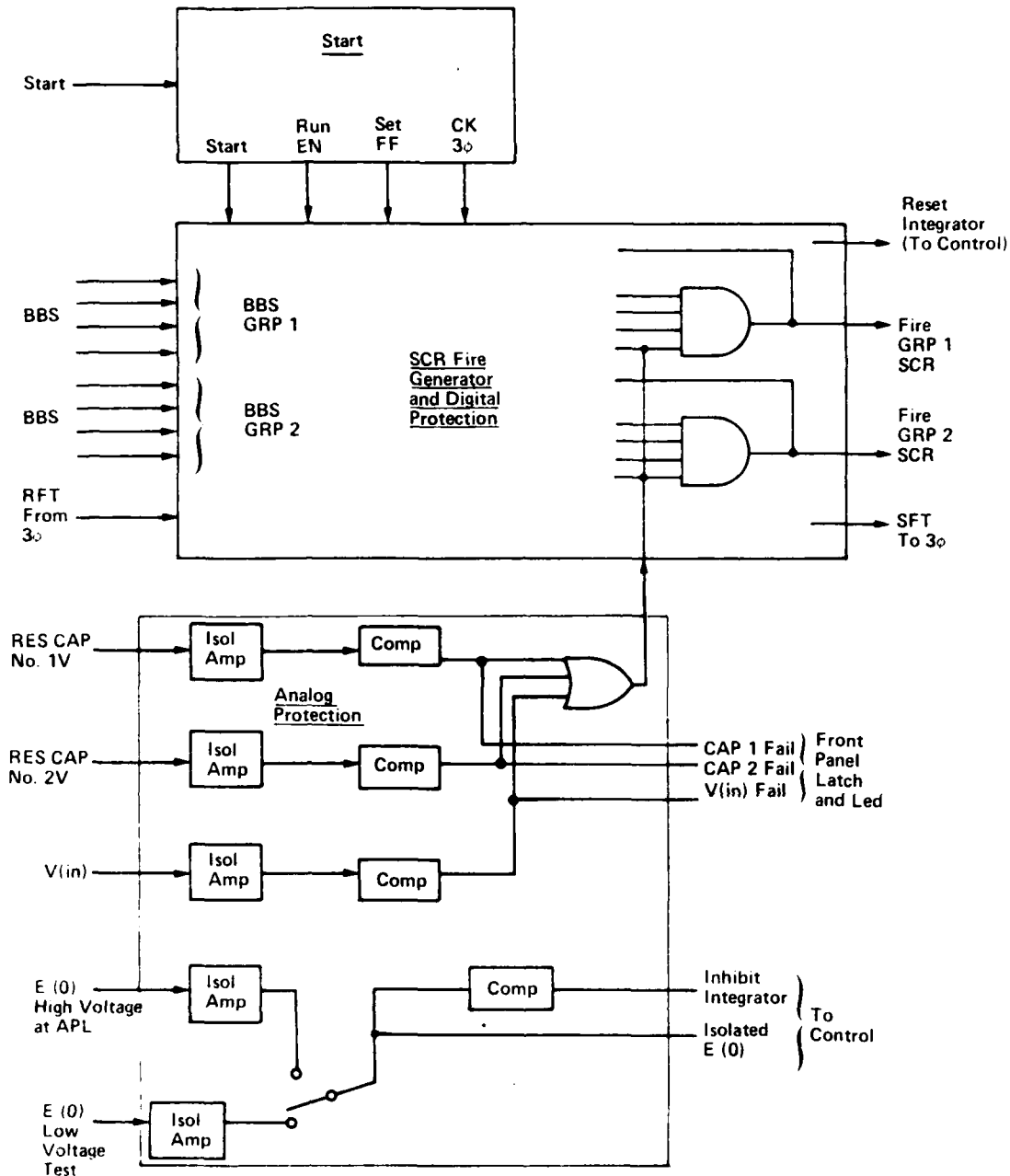


Figure 2.5.3-1 Protection-Simplified Block Diagram

2.5.3.2.1 SCR Fire Generator and Digital Protection - This circuit will generate alternate SCR fire signals; fire GRP1 SCR, Fire GRP2 SCR, and then repeat. The logic expression for fire SCRs is

$$\text{Fire GRP 1 SCR} = (\text{FIRE}) \cdot (\overline{\text{ANALOG PROTECT}}) \cdot (\overline{\text{TOGGLE FF}})$$

$$\text{Fire GRP 2 SCR} = (\text{FIRE}) \cdot (\overline{\text{ANALOG PROTECT}}) \cdot (\overline{\text{TOGGLE FF}})$$

After a fire command has been issued, the circuit will check to see that a valid back bias signal has been received from the last fired group of SCKs. For example, if GRP 1 was last fired, there will be a valid back bias signal from GRP 1 BBS before GRP 2 SCRs can be fired. The back bias signal will exist for TQ seconds before it is considered valid.

The following is a description of the requirements for responding to RFT and generating SFT when the protection unit is used in the three-phase system. When RFT is true, the fire flip flop will not issue a fire signal. The system will wait until both Fire GRP 1 SCR and Fire GRP 2 SCR signals are false, and then it will look for a back-bias to forward-bias transition on BBS 1 or BBS 2. When it finds the back-to-forward bias transition, the circuit will send a SFT to the three-phase unit.

2.5.3.2.2 Start Circuit Requirements - An external OFF/RUN switch with debounce circuits will be provided. The following requirements for a start sequence are established:

- 1) Main power disconnected;
- 2) RUN/OFF switch to OFF;
- 3) Bias supply to ON; external pause to ensure bias supply output in steady state;
- 4) Main power connected;
- 5) RUN/OFF switch to RUN.

Three sets of requirements must be addressed: (1) OFF requirements, (2) RUN requirements, and (3) STOP requirements.

2.5.3.2.3 OFF Requirements - Under the constraints that main power must be disconnected, RUN/OFF to OFF, and then the bias supplies are turned on, the following requirements are established:

- 1) START will be false;
- 2) Hold the following flip-flops in the reset state;
 - a) Start flip-flop;
 - b) Memory latch;
 - c) Fire flip-flop;

Holding START false ensures that no Fire GRP 1 or 2 SCR signal can be issued. Holding the three flip-flops (FFs) in reset for an OFF switch command ensures they are in the proper initial state when a RUN command is received.

2.5.3.2.4 RUN Requirements - The proper initial states were established during the OFF state by resetting the Start FF, Memory Latch, and Fire FF. When the RUN/OFF switch goes to RUN, the following sequence will occur:

- 1) Remove reset to Start FF, Memory Latch, and Fire FF;
- 2) Use a one shot to provide a pulse to SFT;
- 3) Use the 1-0 edge of SFT to clock the Start FF;
- 4) The Start FF will set the Fire FF.

The start circuit will only pulse one group of SCRs, GRP 1 or GRP 2. The initial group of SCRs to be turned on will be chosen based on the polarity of the resonant capacitor. The SCRs will be chosen so the resonant capacitor voltage adds to the source voltage. When either Fire Group 1 or 2 SCRs is True, the Start FF will be reset to remove the set command to the Fire FF. The start circuit will have no further effect on the system after one group of SCRs has been fired once.

2.5.3.2.5 STOP Requirements - The STOP requirement provides for safe turn-off of the power stage by the RUN/OFF switch while main power is connected.

The STOP requirements are satisfied for all three power units. For the two dc/dc units, when the RUN/OFF switch goes to OFF, the Fire Group 1 and 2 SCR signals are held false. The commutating diodes provide a path for the resonant current. For use with the three-phase units, when the RUN/OFF switch goes to OFF, the Fire Group 1 and 2 SCR commands are inhibited. In the three-phase unit, the SCRs that are to be used as diodes are controlled only by the V12, V13, V23, and BBS signals. Thus, the commutating diode function will be provided even though the Fire signal is driven false.

2.5.3.2.6 Analog Protection Requirements - Table 2.5.3-2 identifies the analog input signal names and characteristics for each of the three power units. There are different analog inputs for the three different power units. In all cases, the resonant capacitor voltage can have a common-mode voltage equal to the source voltage. The resonant capacitors all have a maximum operating voltage limit. This protection limit must be set lower than the nameplate rating. When the protection limit is exceeded, the capacitor will be protected by inhibiting SCR fire commands. Because the resonant capacitor voltage can swing both plus and minus, a window comparator will be required.

Source voltage is to be sensed, compared to a positive limit only, and the SCR fire commands stopped if the input limit is exceeded.

Table 2.5.3-2 Analog Inputs to Protection from the Three Power Units

Power Unit	Inputs	Common-Mode Voltage	Limits	Ground Reference
10 kW dc-dc 1/2 Bridge	Resonant Cap V V(IN) dc E(OUT) Flight E(OUT) Test	600 V 2 V 2 V 250 V	+750 V 700 V 5 V + TBD 350 V	Input Input Output Input
5 kW ac-dc Full Bridge	Resonant Cap V V(IN) Rectified Three-Phase E(OUT) Flight E(OUT) Test	300 V 2 V 2 V 250 V	+600 V 200 V 7 V 350 V	Input Input Output Input
200 kW dc-dc Twin Full Bridge	Bridge 1 Resonant Cap V Bridge 2 Resonant Cap V V(IN) E(OUT) Flight E(OUT) Test	600 V 600 V 2 V 2 V 600 V	+750 V +750 V 700 V 7 V 650 V	Input Input Input Output Input

For each of the three power units, E(OUT) is available in two configurations. In the flight configuration, there will be an isolation transformer between input and output. The sensed output voltage will be 5 V for full scale. The isolation requirements are 1 megohm at 2 V common mode at dc. When used, it is required that the power return, signal return, and output return all be connected to a single-point ground. When the sensed output voltage exceeds a limit, the integrator in the control unit is inhibited. A configuration used for test only, has no output transformer for the power stage. The primary of the output transformer is replaced by a diode bridge, filter capacitor, and resistive load.

2.5.3.3 Block Diagram - Figure 2.5.3-1 is a simplified block diagram of the protection unit. All input and output signals for the protection unit are identified in the figure. All logic signals are positive true. The start signal will be externally debounced.

2.5.3.4 Schematic Diagram - Figure 2.5.3-2 is a schematic diagram for the protection unit.

2.5.3.5 Power Requirements - The protection unit will be supplied with + and -15 V \pm 10%. The power dissipation will be less than 0.5 W.

2.5.3.6 Parts List - Table 2.5.3-3 gives the parts list.

Table 2.5.3-3 Protection Unit Parts List

Reference Designator	Part Number	Description
U1	CD4538BE	Dual Monostable
U2, U3	CD4013BE	Dual D Flip-Flop
U4	CD4049BE	Hex Inverter
U5, U11, U12	CD4071BE	Quad 2 Input or
U6, U7, U8	CD4073BE	Jual JK Flip-Flop
U10	CD4028BE	Quad 2 Input and
U13, U14	LM124	Quad Operational Amp
U15, U21	LM111J	Comparator
UR1	LM129A	Reference Diode

2.5.4 Three-Phase Unit

2.5.4.1 Background - Figure 2.5.4-1 shows the topology of the existing three-phase power stage. There are six pairs of oppositely connected SCRs, or a total of 12 SCRs. A representation of the input three-phase, sinusoidal waveforms is at the top of Figure 2.5.4-2 (Ref 7). A simplified explanation of the three-phase unit's requirements follows. It is necessary to select the phase pair that has the largest positive difference. In 360 electrical degrees, there will be six phase pairs. Each phase pair will be 60 electrical degrees long, or last 2.8 ms for a 60-Hz input. When the power stage is within the time period of a phase pair, it uses only four SCR pairs and operates as a conventional full-bridge SRI. This is illustrated in Figure 2.5.4-3.

As the phase pairs change, the selection of four out of the six SCR pairs changes. Each SCR not used 1/3 of the time, is used as an SCR for another 1/3 of the time, and is used as a diode for 1/3 of the time.

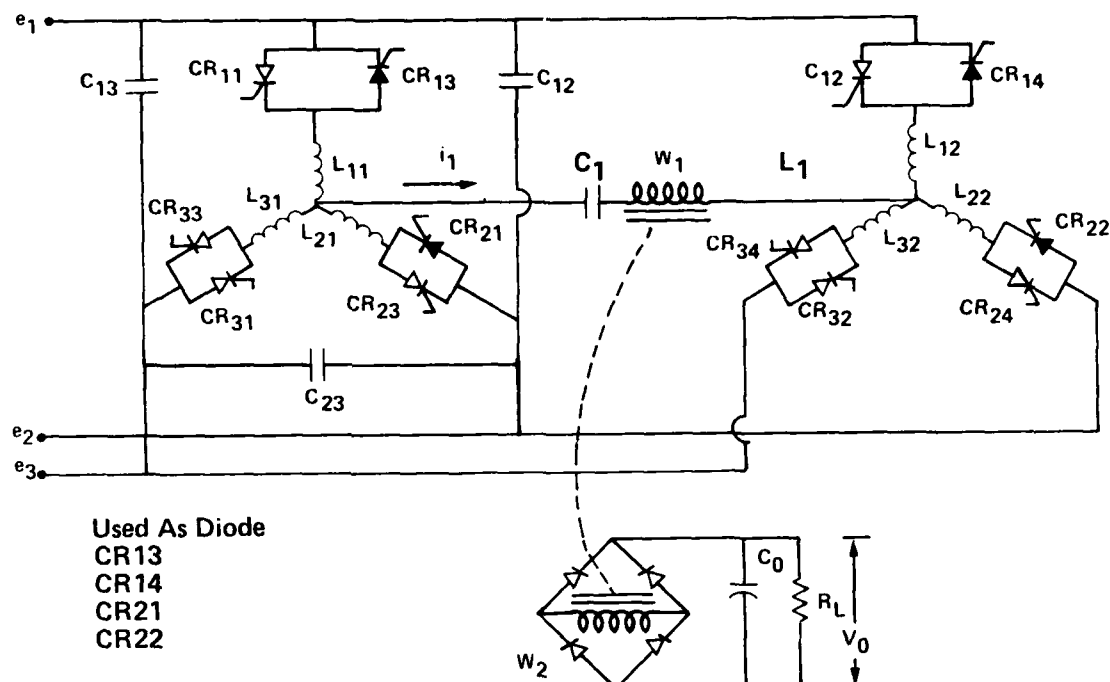


Figure 2.5.4-1 Three-Phase ac-dc SRI-Based Converter, 5 kW ac-dc

2.5.4.2 Requirements

2.5.4.2.1 Logic Requirements - Table 2.5.4-1 summarizes the high-level requirements for the three-phase unit.

Table 2.5.4-1 Three-Phase Unit Top-Level Requirements

-	Determine phase pair.
-	Determine the proper back-bias states based on the phase pair.
-	Generate 12 SCR fire signals based on the phase pair and a fire group 1 or 2 SCR signal from the protection unit (when the SCR is used as an SCR).
-	Generate 12 SCR fire signals based on the phase pair and the back-bias states (when the SCR is used as a diode).

The logic requirements for the three-phase unit are derived from the topology of the existing three-phase unit and the three-phase signal diagram. Figure 2.5.4-2 (Ref 7) shows the three-phase signals where e_1 , e_2 , and e_3 are the three-phase inputs. V_{12} , V_{13} , and V_{23} determine whether a particular phase is positive or negative with respect to another phase voltage and each is positive for 180 out of 360 electrical degrees. The Φ_{1-2} to Φ_{3-2} pick the instantaneous phase pair with the maximum positive difference. Each of the six Φ s is true for 60 out of 360 electrical degrees.

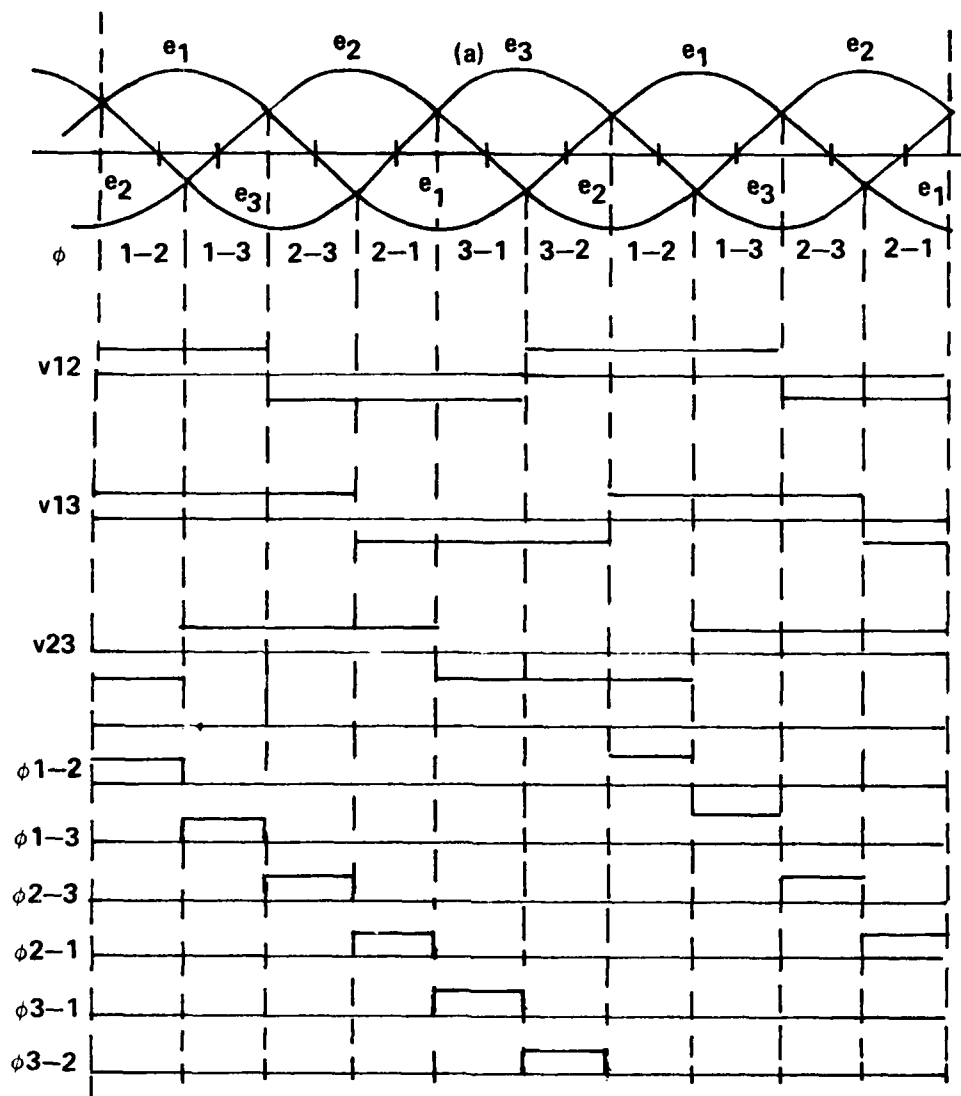


Figure 2.5.4-2 Three-Phase Signals from Schwartz (Ref 7)

Figure 2.5.4-1 shows the topology of the existing APL three-phase power stage. Figure 2.5.4-3 shows the eight SCR's that are active for Phi 1-2.

The SCR's used as diodes in Phi 1-2 have been highlighted in black. Four SCR's are not used in Phi 1-2. Five more schematics similar to Figure 2.5.4-3 could be drawn and the active devices identified to function as an SCR or a diode. Using Figure 2.5.4-2 for Phi 1-2 and five similar figures for the other five phase pairs, one can derive the use of each SCR by phase pair. Each SCR is identified by designator and function (SCR or diode) in each of the six phase pairs in Table 2.5.4-2. In the table, S represents use as an SCR and D represents use as a diode. While Phi 1-2 exists for 60 electrical degrees, the unit functions as a full-bridge SRI. For resonant current of one direction, SCR11 and SCR24 function as SCR's and SCR13 and SCR22 are used as their

antiparallel diodes. For resonant current of the opposite polarity, SCR23 and SCR12 are used as SCRs and SCR21 and SCR14 are used as anti-parallel diodes.

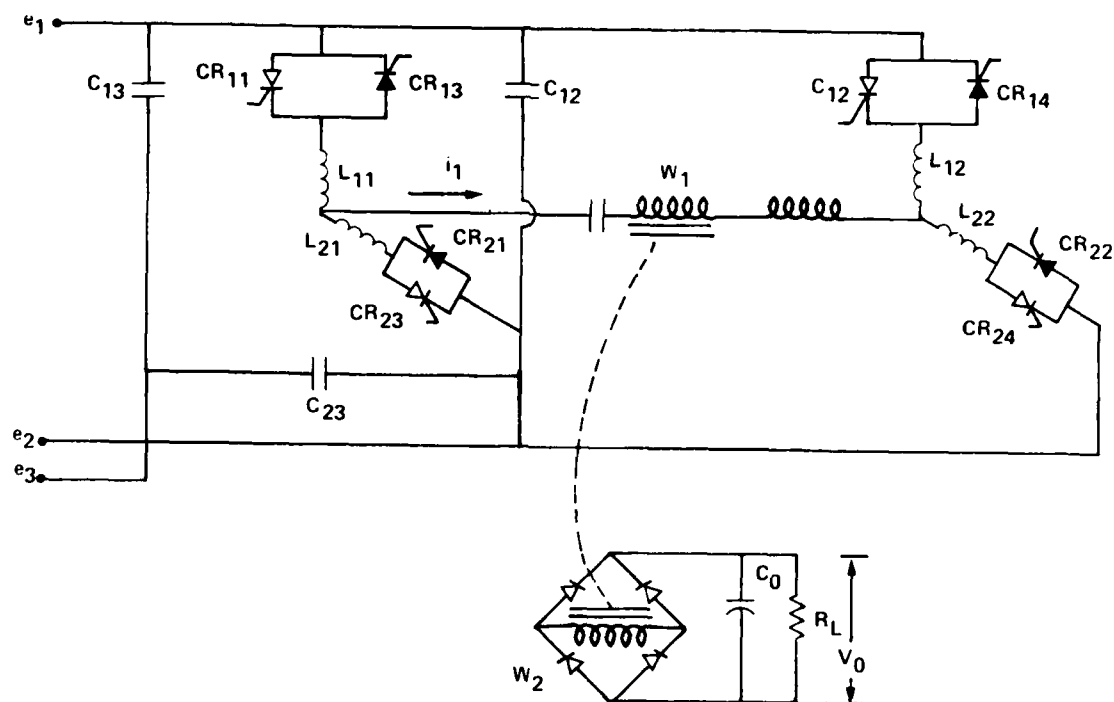


Figure 2.5.4-3 Three-Phase, $e_1 > e_2$, Φ_{1-2}

The logic signal requirements derivation is now reduced to defining the logic equations for:

- 1) V12, V13, and V23;
- 2) RFT;
- 3) Generate six Φ_{XY} from V12, V13, and V23;
- 4) Group 1 and Group 2 Enable (back-bias check);
- 5) 12 SCR commands (both as SCR and diode).

2.5.4.2.2 V12, V13, and V23 Generator - The generator is shown in Figure 2.5.4-4. Comparators U1, U2, and U3 are used to generate V12, V13, and V23 from the phase voltages. The logic for V12, V13, and V23 is tabulated:

Phase Voltages	V(iJ)
$e_1 > e_2$	V12 High
$e_1 < e_2$	V12 Low
$e_1 > e_3$	V13 High
$e_1 < e_3$	V13 Low
$e_2 > e_3$	V23 High
$e_2 < e_3$	V23 Low

Table 2.5.4-2 SCR Identified by Phi and Use (SCR or Diode)

Φ	SCRs											
	11	13	21	23	31	33	12	14	22	24	32	34
1-2	S									S		
		D							D			
1-3	S											S
		D									D	
2-3			S									S
				D							D	
2-1			S									
				D								
3-1					S			S				
						D					S	
3-2					S				S			
						D			D		S	

The three flip-flops U4, U5, and U6 are used to hold the three states, clock them, and generate the inverse states.

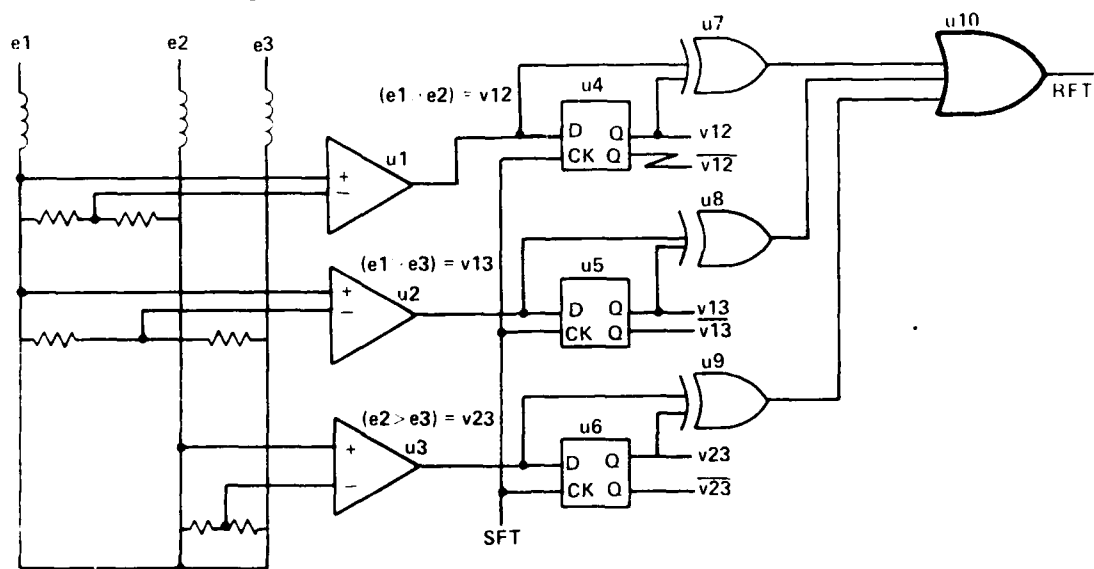


Figure 2.5.4-4 VXY and RFT Generator

2.5.4.2.3 RFT Generator - Figure 2.5.4-4 is a simplified schematic of the RFT generator. The generator comprises the three D flip-flops (U4 to U6), the three EXCLUSIVE OR gates, U7 to U9, and the OR gate U10. It is necessary to generate an RFT (Request for transition) signal whenever a D flip-flop input is different from its Q output. The expression for RFT is a logic equation. The logic symbolism used is tabulated.

<u>Description</u>	<u>Logic Symbol</u>
Logical OR	+
Logical AND	·
Exclusive OR	⊕
Logic Variable	A
NOT A	\overline{A}
N th D FF Input	ND
N th D FF Q Output	NQ
N th D FF Q NOT Output	\overline{NQ}

The logic equation for RFT is

$$1) \dots RFT = (4D + 4Q) + (5D + 5Q) + (6D + 6Q).$$

The implementation for RFT from (1) requires a three-input OR gate. It is desirable to replace the OR gate with a NAND gate for versatility.

To derive the NAND implementation, logically negate RFT twice and then apply DeMorgan's theorem to obtain

$$2) \dots RFT = \overline{1D \oplus 1Q \cdot 2D \oplus 2Q \cdot 3D \oplus 3Q}.$$

Using Boolean algebra, it can be shown that

$$3) \overline{D \oplus Q} = D \oplus \overline{Q},$$

and by substitution in Equation 2, RFT becomes

$$4) \dots RFT = (1D \oplus \overline{1Q}) \cdot (2D \oplus \overline{2Q}) \cdot (3D \oplus \overline{3Q}),$$

which can be implemented by three two-input EXCLUSIVE OR gates and a three-input NAND gate.

RFT is an input to the protection circuit. The protection circuit requirements to generate a SFT (safe for transition) signal are:

- 1) Inhibit any SCRs from firing;
- 2) Allow SCRs used as diodes to fire;

- 3) Wait until SCRs used as diodes have stopped conducting (no back-bias signals exist);
- 4) Delay for TQ to allow SCK used as diode to recover blocking capability.

The SFT signal from the protection circuit will be used to clock the three D flip-flops.

2.5.4.2.4 Phi XY Generator - The six Phi ij logic equations can be written directly from the three-phase signal chart in Figure 2.5.4-2. Table 2.5.4-3 shows the six logic equations for the Phi ij. Table 2.5.4-4 shows the definitions of the Group 1 and 2 SCRs.

Table 2.5.4-3 Logic Equations for Phi 12 to 32

$\text{PH1 } 12 = \text{V12.V13.}\overline{\text{V23}}$
$\text{PH1 } 13 = \text{V12.V13.V23}$
$\text{PH1 } 23 = \overline{\text{V12.V13.V23}}$
$\text{PH1 } 21 = \overline{\text{V12.V13.V23}}$
$\text{PH1 } 31 = \overline{\text{V12.V13.V23}}$
$\text{PH1 } 32 = \text{V12.}\overline{\text{V13.}\overline{\text{V23}}}$

Table 2.5.4-4 Definition of Group 1 and 2 SCRs

<u>Group 2 SCRs</u>	<u>Group 1 SCRs</u>
SCR11	SCR23
SCR24	SCR12
SCR34	SCR33
SCR21	SCR22
SCR14	SCR13
SCR31	SCR32

2.5.4.2.5 Group 1 Enable and Group 2 Enable - Group 1 Enable and Group 2 Enable are generated in the three phase unit and sent to the protection unit. For operating the SRI, there are two groups of SCRs. They are fired alternately. Before Group 1 SCK can be fired, it is necessary to ensure all of the Group 2 SCRs are off (back-biased). Also,

before a Group 2 SCR can be fired, it is necessary to ensure all Group 1 SCRs are back-biased.

The logic equations for GRP 1 Enable and GRP 2 Enable can be written by inspection from Table 2.5.4-2.

The definition of Group 1 and Group 2 SCR depends on the Φ_{ij} .

From Table 2.5.4-2, before SCR23 and SCR12 can be fired as SCRs, there must be back bias signals for SCR11 and SCR24. In all the phases, the top pair used as SCRs is called Group 1 and the bottom pair Group 2. By inspection from Table 2.5.4-2:

$$\begin{aligned} \text{GRP 2 EN} = & (\Phi_{12}) \cdot (\text{BBS } 11) \cdot (\text{BBS } 24) + (\Phi_{13}) \cdot (\text{BBS } 11) \cdot (\text{BBS } 34) \\ & + (\Phi_{23}) \cdot (\text{BBS } 21) \cdot (\text{BBS } 34) + (\Phi_{21}) \cdot (\text{BBS } 21) \cdot (\text{BBS } 14) \\ & + (\Phi_{31}) \cdot (\text{BBS } 31) \cdot (\text{BBS } 14) + (\Phi_{32}) \cdot (\text{BBS } 31) \cdot (\text{BBS } 24) \end{aligned}$$

$$\begin{aligned} \text{GRP 1 EN} = & (\Phi_{12}) \cdot (\text{BBS } 23) \cdot (\text{BBS } 12) + (\Phi_{13}) \cdot (\text{BBS } 11) \cdot (\text{BBS } 34) \\ & + (\Phi_{23}) \cdot (\text{BBS } 21) \cdot (\text{BBS } 34) + (\Phi_{21}) \cdot (\text{BBS } 13) \cdot (\text{BBS } 22) \\ & + (\Phi_{31}) \cdot (\text{BBS } 11) \cdot (\text{BBS } 32) + (\Phi_{32}) \cdot (\text{BBS } 23) \cdot (\text{BBS } 32) \end{aligned}$$

GRP 1 EN is of the AND/OR logic form. The function can be implemented with six 3-input AND gates and a 6-input OR gate. To save on gate inventory, it is convenient to convert the AND/OR logic to NAND/NAND to allow implementation with a single type of gate. To convert to NAND/NAND, use the following identity

$$F = A \cdot B + C \cdot D = \overline{\overline{A \cdot B + C \cdot D}} = \overline{(\overline{A \cdot B}) \cdot (\overline{C \cdot D})}$$

The output will be positive true.

Two of the design constraints from CRM for radiation-hard design are (1) eliminate 8 input AND gates and (2) replace NOR logic with NAND.

There is no NOR logic, but there could be an 8-input NAND in GRP 1 and 2 EN. To follow the CRM constraints, the GRP 1 and 2 EN will be implemented without an 8-input NAND. GRP 1 and 2 EN will be implemented with 3-input NAND gates only. The implementation is shown in Figure 2.5.4-5.

2.5.4.2.6 SCK Fire Commands - The logic equations can be written directly from Table 2.5.4-2. Because there are 12 SCRs, 12 logic equations are required. Firing the SCR when it functions as both an SCR and as an antiparallel diode must be accounted for. For example, SCR11 is used as an SCK in Φ_{12} and Φ_{13} , and is used as a diode in Φ_{21} and Φ_{31} . Fire Group 1 and Fire Group 2 are generated in the protection unit and are inputs to the three phase unit.

The logic equation for firing SCR11 can be written as

$$\begin{aligned} \text{FIRE SCR11} = & (\text{FIRE GRP 2}) \cdot (\Phi_{12} + \Phi_{13}) \\ & + (\text{BBS } 13) \cdot (\Phi_{21} + \Phi_{31}). \end{aligned}$$

A simplification can be made if the OR of two Phis is expressed in terms of the V12, V13, and V23. Using the three-phase signal definitions from Figure 2.5.4-2, the FIRE SCR11 logic equation can be reduced to

$$\text{FIRE SCR11} = (\text{FIRE GRP 2}) \cdot \text{V12} \cdot \text{V13} + (\text{BBS 1-3}) \cdot \overline{\text{V12}} \cdot \overline{\text{V13}}.$$

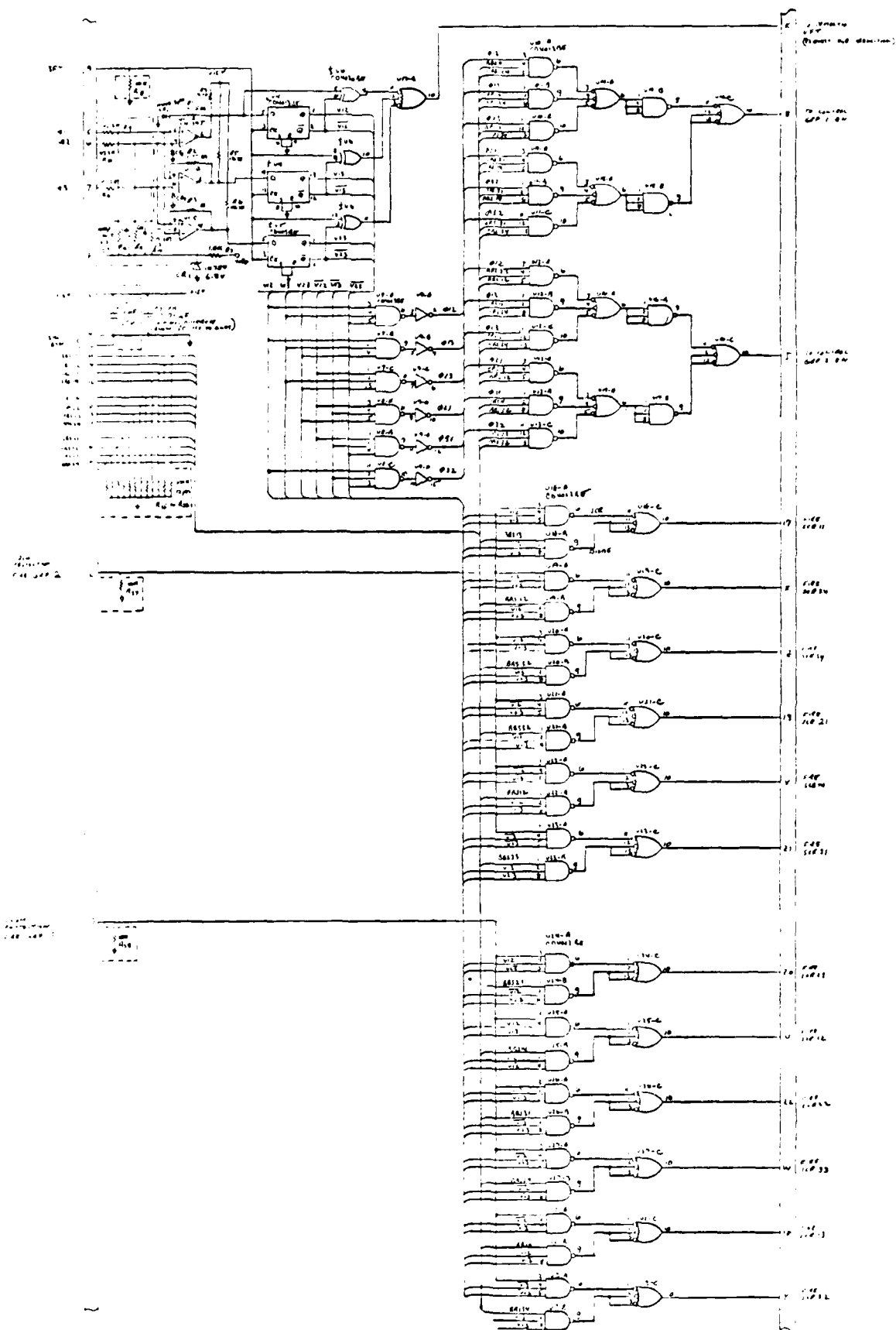


Figure 2.5.4-5 Three Phase Unit Schematic

The other 11 FIRE SCR logic equations all have the same form. Table 2.5.4-5 shows all 12 fire SCR logic equations.

Table 2.5.4-5 Fire Logic Equations

FIRE Group 1 = FG 1 and FIRE Group 2 = FG 2
FIRE SCR11 = $FG2 \cdot V12 \cdot V13 + BBS\ 13 \cdot \overline{V12} \cdot \overline{V13}$
FIRE SCR24 = $FG2 \cdot V12 \cdot \overline{V23} + BBS\ 22 \cdot \overline{V12} \cdot V23$
FIRE SCR34 = $FG2 \cdot V13 \cdot V23 + BBS\ 32 \cdot \overline{V13} \cdot V23$
FIRE SCR21 = $FG2 \cdot \overline{V12} \cdot V23 + BBS\ 23 \cdot V12 \cdot \overline{V23}$
FIRE SCR14 = $FG2 \cdot \overline{V12} \cdot \overline{V13} + BBS\ 12 \cdot V12 \cdot V13$
FIRE SCR31 = $FG2 \cdot \overline{V13} \cdot \overline{V23} + BBS\ 33 \cdot V13 \cdot V23$
FIRE SCR23 = $FG1 \cdot V12 \cdot \overline{V23} + BBS\ 21 \cdot \overline{V12} \cdot V23$
FIRE SCR12 = $FG1 \cdot V12 \cdot V13 + BBS\ 14 \cdot \overline{V12} \cdot \overline{V13}$
FIRE SCR33 = $FG1 \cdot V13 \cdot V23 + BBS\ 31 \cdot \overline{V13} \cdot \overline{V23}$
FIRE SCR22 = $FG1 \cdot \overline{V12} \cdot V23 + BBS\ 24 \cdot \overline{V12} \cdot \overline{V23}$
FIRE SCR13 = $FG1 \cdot \overline{V12} \cdot \overline{V13} + BBS\ 11 \cdot V12 \cdot V13$
FIRE SCR32 = $FG1 \cdot \overline{V13} \cdot \overline{V23} + BBS\ 34 \cdot V13 \cdot V23$

The form of the fire SCR logic equations is AND/OR. It is more convenient to implement the logic with only NAND gates. To convert the AND/OR logic to NAND/NAND logic, use the identity

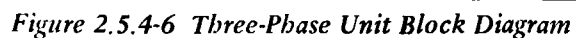
$$F = A \cdot B + C \cdot D = \overline{(\overline{A \cdot B}) \cdot (\overline{C \cdot D})}.$$

When converted to the NAND/NAND form, the logic equation for FIRE SCR11 becomes

$$FIRE\ SCR11 = (FG2 \cdot V12 \cdot V13) \cdot (BBS12 \cdot \overline{V12} \cdot \overline{V13}).$$

Figure 2.5.4-5 shows the NAND/NAND implementation of the 12 FIRE SCR logic equations from Table 2.5.4-5.

2.5.4.4 Block Diagram - Figure 2.5.4-6 is a block diagram of the three-phase unit. All of the input and output signals for the three-phase unit are shown. All logic signals are positive true and will be compatible with CMOS powered from 15 V.



2.5.4.6 Parts List - The parts list is shown in Table 2.5.4-6.

Table 2.5.4-6 Three-Phase Unit Parts List

Reference Designator	Part Number	Description
U1	LM 139J	Quad Voltage Comparator
U2, U3, U7, U10 - U27	CD 4023 BE	Triple Three-Input NAND Gate
U4, U5	CD 4013 BE	Dual D Flip-Flop
U6	CD 4030 BE	Quad 2 Input EX OR
U9	CD 4049 BE	Hex Inverter

2.5.5 Control Unit

2.5.5.1 Background - The control unit requirements for the three existing APL converters were established. The 10 kW dc-dc unit had a current control loop, but not a voltage control loop. The 5-kW ac-dc unit had both a voltage and a current control loop. The 200-kW unit had a current control loop.

For a general control unit applicable to a wide range of SRI topologies, it is necessary to implement both a fast current control loop and a slower voltage control loop. The two feedback variables are the resonant current and the output voltage. The basic control in the three units consists of integrating a portion of the rectified resonant current, comparing the integrator output to a reference, and sending an SCR fire signal when the integrator output exceeds the reference. In the 10 kW unit, only the diode portion of the resonant current is integrated. The basic relations among the rectified resonant current, reset, integrator output, and fire command--are shown in Figure 2.5.5-1.

In Figure 2.5.5-1, only the diode portion of the resonant current is integrated. When the integrator output exceeds the reference, a fire command to the protection unit is issued. When the protection unit declares that it is safe to fire the SCRs, it first fires the SCRs and then generates a reset to the integrator. The fire signal must be latched in the protection unit. From the figure it is apparent that the resonant current cannot be integrated directly; an increase in diode current causes a decrease in the SCR firing angle that results in a larger resonant current. The simplest stable current control loop is one where the resonant current is subtracted from a reference and the difference is integrated.

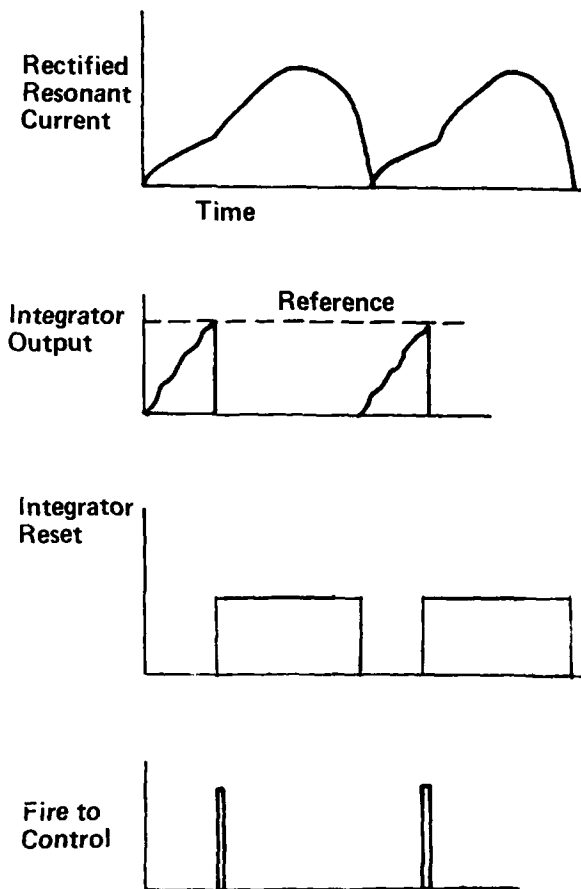


Figure 2.5.5-1 Control Unit Waveform

One additional function must be incorporated: an integrator inhibit function. Integrator inhibit is used to hold the integrator and stop it from integrating. This function effectively removes the input to the integrator but does not reset it. Output voltage is used as the parameter to control integrator inhibit. When the output voltage exceeds a limit, the integrator will be inhibited.

2.5.5.2 Requirements - The feedback variables will be the resonant current and the output voltage. The resonant current will be rectified in the control unit and there will be both a current and a voltage control loop. The output voltage will be compared with a reference and the error voltage integrated in the first integrator. This integrator time constant is expected to be several half periods of 10 kHz. The difference between the output of the first integrator and the resonant current will be the input to the second integrator. The time constant of the second integrator will be determined from the breadboard and is expected to be close to a half period of 10 kHz. The output of the second integrator will be compared with a reference and when the reference is exceeded, a fire command will be issued. Two positive true logic commands will be incorporated in the control unit. The reset

signal will reset the second integrator to a known voltage. The inhibit command will remove the input to the integrator. All interface signals will be compatible with 15-V CMOS.

2.5.5.3 Block Diagram - Figure 2.5.5-2 is a block diagram of the control unit. This block diagram mechanizes the requirements described in the previous section. A significant feature of this implementation is the second integrator, which is discussed next.

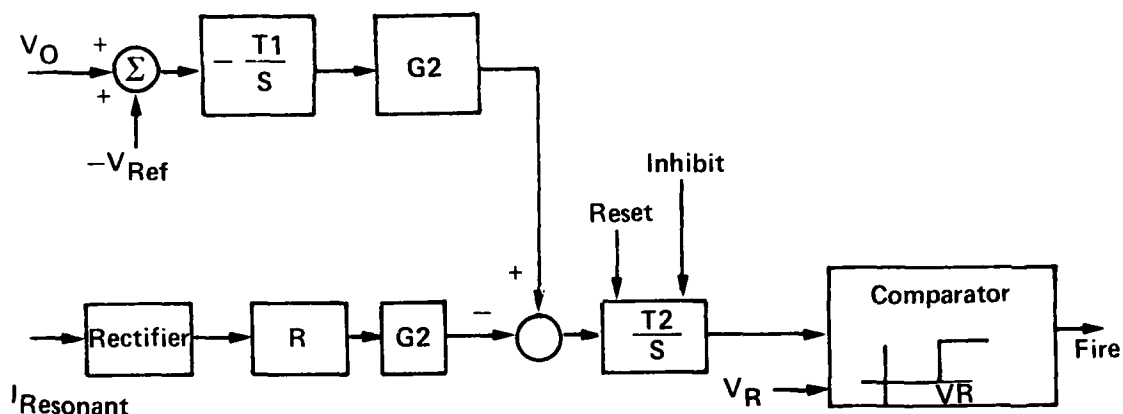


Figure 2.5.5-2 Control Unit Block Diagram

The output of the integrator is compared with reference voltage T_{wo} , and a fire SCR command is issued when the reference is exceeded. The following comments about the form of the integrator output are pertinent. First, when the system is initially turned on, $e(out)$ and the resonant current are both zero. Because the reference voltage T_{wo} is not zero, the output of integrator Two will rapidly go to the reference level and a fire command will be generated. In the steady-state, an increase in the resonant current will result in the integrator taking longer to reach the reference level T_{wo} where a fire command is issued. Similarly, a decrease in $e(out)$ will increase the SCR firing angle. The system is stable on a cycle-by-cycle basis.

2.5.5.4 Circuit Diagram - A control unit circuit schematic is shown in Figure 2.5.5-3.

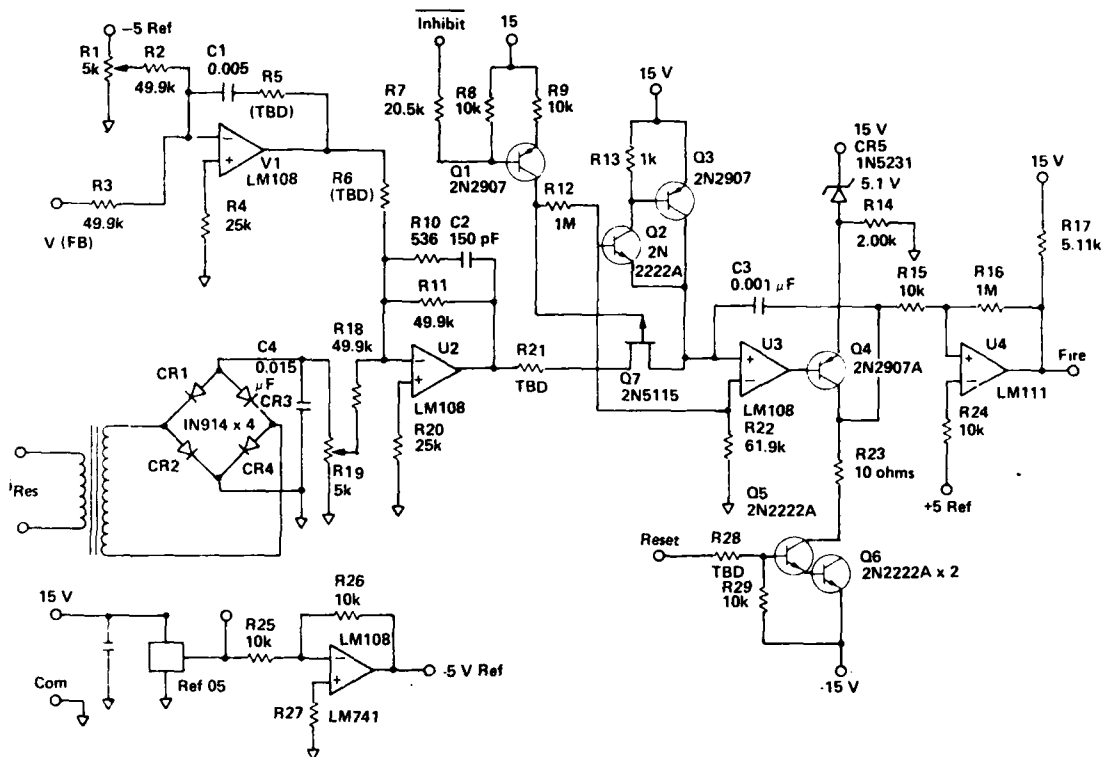


Figure 2.5.5-3 Control Unit Schematic

2.5.5.5 Power - The control unit will be supplied with $\pm 15\text{ V} \pm 10\%$. The $+15\text{ V}$ will be the same as is used for the 15-V CMOS logic in the protection unit.

2.5.5.6 Parts List - Table 2.5.5-1 is a parts list.

Table 2.5.5-1 Control Unit Parts List

Reference Designator	Description	P/N
U1, U2, U3, U5	Operational Amplifier	LM108A
U4	Comparator	LM111A
Q1, Q3, Q4	PNP	2N2907A
Q2, Q5, Q6	PNP	2N2222A
Q7	P Channel FET	2N5115

2.6 MICROPROCESSOR STUDY

2.6.1 Study Guidelines

The first reason to consider a microprocessor was to make it easier to reconfigure the controller for operation with the three existing power sections. The second was to identify candidate tasks for a microprocessor in future SRI-based converters.

2.6.2 Microprocessor Reconfiguration Study

A study was performed to identify how a microprocessor could be used to reconfigure the controller to make it easier to use with the three existing APL power sections. The block diagrams of the controller for each of the power stages were inspected, and the most complex controller was for the three-phase ac-dc unit. The following scenario was used for the study. The most complex controller, the 5-kW ac-dc, would be fabricated first. There would be one controller panel for BNC cable interfaces. When configurations were changed, cables from the controller BNC cable interface to a different power unit would be changed. For the microprocessor to reconfigure the control system, analog switches or relays would have to be added along with interface circuits. The switches could be used to change interconnections among the controller blocks to connect the three-phase controller for the ac-dc unit or to disconnect it for dc-dc control. The switches could also be used to change the following gains:

- 1) Differential amplifiers for resonant capacitor voltages;
- 2) Resonant current transformer amplifiers;
- 3) Source voltage;
- 4) Output voltage amplifier.

The operator could give one command to the microprocessor to change the switches from one configuration to the next. This is the only function for the microprocessor. The microprocessor would not operate again until the next time the operator wanted to run the controller with a different power unit. This same function however could be performed by a three-position rotary switch and does not warrant the use of a microprocessor for the following reasons:

- 1) There is no advantage for a microprocessor in configuring a controller. If switches or relays were used for gain and configuration change, the control would be more simply done with the switch rather than a microprocessor;
- 2) A microprocessor would add unnecessary complexity to verify the position of the switches;
- 3) A microprocessor could add unreliability because of transient phenomena that could reconfigure the controller while the power stage was running; this would have a potentially disastrous impact on the power stage;

- 4) A microprocessor would require an UPS to remove facility power transients.

2.6.3 Microprocessor Functions for Future SRI

The purpose of this study was to also identify areas of applying microprocessors in future SRI-based converters.

The methodology for performing this study was to identify failure modes and effects, a measurements list and microprocessor functions.

Table 2.6-1 (Ref 8) summarizes the major failure modes and effects in an SRI. A major failure mode is a shorted SCR. When an SCR shorts, there will be a short across the source the next time its companion SCR fires. This type of fault will normally be cleared by an input fuse opening. The failures fall into three classes:

- 1) No output;
- 2) High or low output voltage;
- 3) SRI overheats.

Table 2.6-1 Series-Resonant Inverter Failure Modes and Effects

Failure Mode	Cause	Effect
Power SCR Short	SCR Fail, Control Failure, Fuse Fail	No Output
Power SCR Open	Control or SCR Fail	No Output
Commutation Diode Shorted	Diode Fail, Fuse Fail	No Output
Load Short	Load Fail	No Output Power, SRI Not Harmed by Short
V (OUT) High	Control Fail, OV Protection Fail	Damage Loads
No Output V	Multiple Component, Wire Open	No Power Output
Degraded Efficiency	Filter Cap ESR Increase	Assembly Overheats
Resonant Caps Fail on Overvoltage	Lack of Redundancy, Lack of Margin	No Output
V(OUT) Low	Control Failure	Insufficient P(OUT)

External failures can also affect the SRI. On the input side, the source voltage can go high or low making it impossible for the SRI to perform its required function. On the output side, the external loads

can fail to low impedance, the output may be overloaded by the system incorrectly connecting an excessive number of loads, or the load bus may open.

A candidate measurements list is shown in Table 2.6-2

Table 2.6-2 Measurements List

Parameter
V(IN)
I(IN)
V(OUT)
I(OUT)
V(Res Cap 1)
V(Res Cap 2)
Temp 1 to Temp N
Resonant Frequency

The measurements include the terminal voltages and currents, resonant capacitor voltages, internal temperatures, and the resonant frequency.

Table 2.6-3 lists the candidate microprocessor functions. The microprocessor is used for automated data acquisition, limit checking, self protection by shutting down when limits are exceeded, state of health monitoring and status reporting, diagnosis and correction of output low voltage conditions, and peak power tracking with a solar array.

A significant microprocessor function is to automate data acquisition and limit checking. By periodically taking the data and comparing them to limits, the SRI state of health can be determined. Measurement of key internal temperatures will be a significant input to state-of-health determination. Efficiency is also a key indicator of state of health. The microprocessor is well-suited to efficiency calculation and limit checking. In general, efficiency will be a function of terminal conditions. As a major problem with power systems in spacecraft in the past has been a paucity of information about real-time failures, one strong automation candidate is failure monitoring and reporting. For example, there can be multiple reasons for low-output voltage. The input voltage may be low, the SRI may have a control failure, or the output may be overloaded. The microprocessor can therefore be used to diagnose the problem and take corrective action. It can be used to check the input for normal values, remove loads on a priority basis and check the output after each removal, or finally diagnose the fault as an internal SRI failure.

Table 2.6-3 Microprocessor Functions for Future SRI

- Data acquisition;
- Perform limit checks on all measurements;
- Self protection by automatic shut down on limit check failure;
- Monitor V(IN), V(OUT), and I(OUT) to sense shorted load; automatically turn SRI off to allow shorted load to be removed or recovered; microprocessor to hold SRI off, then automatically try to restart;
- Monitor key internal temperatures;
- Periodically calculate efficiency and compare to limits; if efficiency is below limits, the microprocessor can report to an operator or the next higher level computer, and system executive can elect to place low efficiency unit on standby and activate back up unit;
- Maintain measurements before and after a shutdown; report reason for shut down along with pre shutdown data to next higher level;
- Maintain a state of health status word for SRI;
- Monitor and report status of input fuse;
- Diagnose reason for low output voltages;
- Perform peak power tracking when power source is a solar array.

2.7 PACKAGING STUDY

In evaluating the 200-kW series-resonant inverter (SRI) design for space-based applications, the packaging design objectives remain essentially the same as in airborne applications; namely, efficient use of materials to minimize weight and volume impact, long-term reliability under all anticipated environments and a design that is producible and maintainable at reasonable cost.

The major differences in design approach result from the environmental factors. The launch and deployment dynamic loads associated with spacecraft missions are generally much more severe than airborne. Random vibration levels for launch are typically in the 10- to 20-grms range for large electronic equipment. The ambient pressure range, lack of gravity effects, and available thermal control methods associated with space operation are even more significant factors influencing the packaging of spaceborne electronics.

To achieve a reliable, efficient design requires a thorough understanding of the environmental effects on the equipment plus a comprehensive knowledge of circuit elements, materials and processes to be employed in packaging the SRI. Figure 2.7-1 shows the twin full-bridge power circuit evaluated for spaceborne packaging considerations.

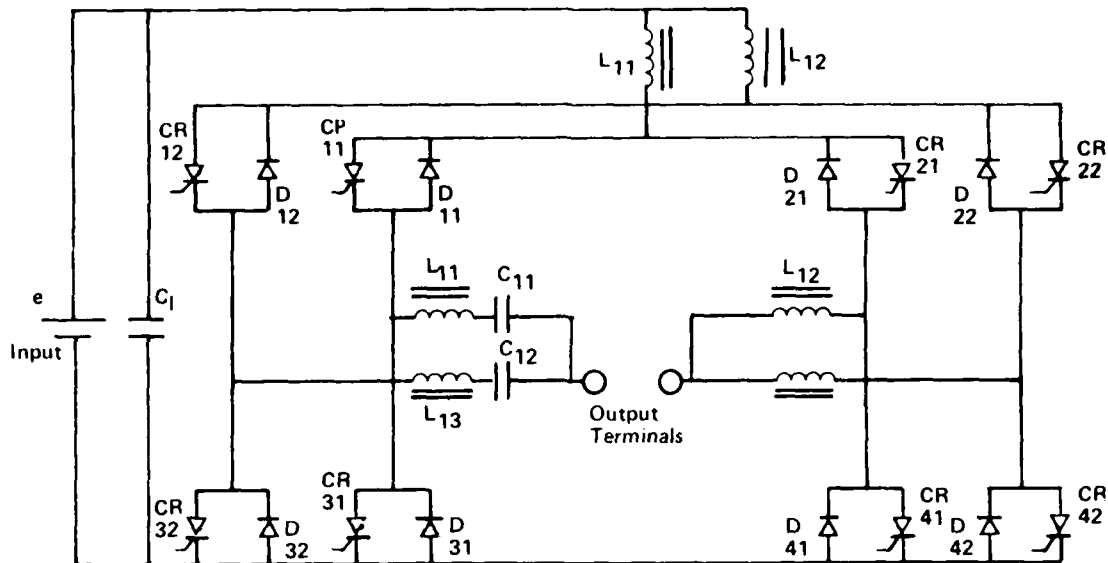


Figure 2.7-1 Power Stage Schematic—200-kW Twin Full-Bridge SRI

The main packaging issues are thermal control, high-voltage protection, structural design, EMI control and power distribution and interconnection.

Table 2.7-1 lists the operational parameters assumed as representative of future space missions for the SRI.

Table 2.7-1 200-kW dc-dc Operational Parameters

Input Voltage	- 200 to 400 Vdc
Output Voltage, Frequency	- 250 V, 10 kHz
Output Power	- 200 kW Max
Power Dissipation	- 8000 W Max
Peak Voltage Stress	- 1000 V at the Series Capacitors
Operating Environmental Pressure	- P 10^{-4} torr, or P 600 torr
Gravity Environment	- 1-g Prelaunch, Zero-g Postlaunch

2.7.1 Thermal Control

The concentrated heat loads dissipated in eight thyristor-diode pairs present a major challenge to the designer. For space operation, thermal conduction paths must be provided to transfer the heat generated from localized sources to a spacecraft radiator designed to efficiently reject thermal energy to deep space. Alternative systems may be used at the spacecraft level to utilize this waste heat in a thermal engine or to absorb thermal energy in an open-loop system, such as a boiler, with vapor ejected to space.

Several methods might also be devised for transporting heat energy from the SRI-localized sources to the spacecraft sink. The heat transfer analysis performed on the 200-kW inverter considered the use of heat pipes as the most efficient and effective method of heat transfer for this application. Heat pipes have been operated successfully as high-conductance devices in spacecraft since 1967. Recent space applications include Skylab, ATS-6 and the STS (space telescope system) scheduled for launch in 1986. Properly designed, heat pipes are considered a highly efficient, reliable method for heat transfer in space operations. The heat pipe uses a boiling-condensing thermal cycle with a small amount of vaporizable fluid contained in a closed tubular structure. Capillary forces pump the fluid to the evaporator where it absorbs heat and vaporizes. The vapor flows along the tube to the condenser section because of a slight pressure difference in that section where heat is rejected through condensation. The process is essentially isothermal except for temperature gradients through the heat pipe structure at the evaporator and condenser sections.

An alternative thermal control system for the SRI heat sources are active cooling loops. A suitable fluid used as a coolant, circulates by electrical pumping to transfer heat loads to the spacecraft sink. The Space Shuttle and Spacelab systems use active coolant loops and cold plates for thermal management of electronic components.

For either passive heat pipes or active coolant loops, thermal impedance must be minimized at mechanical interfaces for concentrated heat loads. For the SRI, maximum thermal flux density occurs at the thyristor contacts, which is estimated to be 26 W/cm^2 . High contact forces and materials to enhance the effective contact area are required to produce acceptable thermal conductions. Similar techniques are required at cold plate interfaces for all major dissipators to maintain effective thermal control.

The 16 SRI power diodes and thyristors may be grouped in a 4×4 array with each device clamped to a common, electrically isolated cold plate base. The eight diode-thyristor pairs are electrically bused together on the cold plate base side using three separate conduction plates according to interconnection requirements of the circuit as shown in the schematic (Fig 2.7-1). A similar arrangement is provided on the opposite side of the thyristor-diode pairs, with four groups of two pairs each connected electrically. Cold plates are attached to each thyristor-diode pair on the top side. This provides cooling from both sides of the disc-shaped semiconductors and facilitates assembly,

test, and repair. This configuration would allow parallel arrays of heat pipes to be attached or embedded in the cold plates, each handling approximately 150 W, assuming four heat pipes per thyristor-diode pair.

The alternative active-coolant-loop scheme may be used in the same manner using suitably designed cold plates attached to coolant loops.

Associated inductors and capacitor banks designed for cold plate mounting may be supported on the cold plate base adjacent to or integrated with the semiconductor array. Additional heat pipes or coolant loops will be required to accommodate the heat load associated with the inductors. The use of multiple heat pipes or coolant loops allows some redundancy without seriously complicating the design.

A dielectric thermal interface material such as fiberglass-reinforced silicon rubber sheet with beryllia or alumina filler is recommended as a candidate material for an interface between the semiconductors and aluminum cold plates.

The cold plates should be designed as an integral extension of the heat pipes or coolant loops to avoid an additional mechanical interface. This will provide a quasi-isothermal cold plate to reduce concentrated hotspots and improve the efficiency of the thermal control system.

Heat pipes have also been successfully integrated into power inductors and transformers to provide efficient thermal conduction paths and eliminate hot spots. In these cases the heat pipes have finned extensions that perform a structural function or act as electrostatic shields and are designed and fabricated into the magnetic assembly. The heat pipes extend from the assembly and are routed to appropriate cold plates or radiator surfaces.

Testing heat pipes in a gravity environment requires the heat pipes be reasonably horizontal to prevent gravity from influencing their capillary pumping ability. This can be accomplished by carefully routing heat pipe elements during design, limiting the array to a single plane, or by ensuring that departures from the plane are designed for a gravity assist during capillary pumping. This is important because inadequate return of condensate to the evaporator section will result in reduced thermal capacity or complete shutdown of the system.

2.7.2 Structural Design

Maximum efficiency will be achieved through using the cold plate component mounting base as the major structural element, with component inertial loads being carried through the cold plate directly to spacecraft supporting structural members. A lightweight vented enclosure designed for EMI control and protection from handling and debris will complete the housing.

Suitable enclosure construction may include formed aluminum sheet-metal covers, aluminum honeycomb constructions, or fiber-reinforced composite enclosures with foil metallization for EMI shielding. The secondary structures required to support the power control electronics and other low dissipating circuits, internal wiring, connectors, and shielding may be machined from aluminum stock and designed for structural continuity to the support base.

The component mounting cold plate with integral heat pipe elements can be considered an efficient plate structure because of its high specific stiffness, similar to corrugated construction. The relatively thick base sections required for thermal conduction can provide structural support to transmit loads to the spacecraft attachment points.

2.7.3 Spacecraft Integration

The obvious choice location for spacecraft mounting of the SRI to minimize weight and facilitate installation and ground testing is centrally on a dedicated radiator panel with the heat pipes routed in a planar array and connected to the radiator elements. In effect, the radiator elements become an extension of the inverter cold plate with heat pipes distributing the thermal load to produce a quasi-isothermal radiating surface.

System efficiency may be further improved by providing dedicated radiator panel elements to handle the heat load from the series inductors because they may be operated at roughly 80°C higher temperatures than the semiconductors. This will allow higher radiator flux densities with some associated weight savings.

For systems employing active cooling loops to remove heat from SRI components, the proximity of the SRI to the radiators is not a major consideration.

2.7.4 High-Voltage Considerations

To achieve reliable operation under widely varying conditions of ground testing and long-term space environments, the numerous factors influencing voltage breakdown in the SRI must be carefully considered. Provision must be made for controlling cracks and voids in insulation to avoid degradation and failure of insulation from partial discharges (Ref 9). The breakdown voltage of a uniform field gap in a gas can be plotted to relate the voltage to the product of gas pressure times the gap length. This is known as Paschen's law. Paschen's law has a minimum breakdown voltage for the critical pressure-spacing product. At 400 Hz the minimum breakdown for air is 327 V peak at the critical pressure spacing product (Ref 10). This voltage is called the corona inception voltage. The spacing and operating pressure must be controlled to ensure the corona inception voltage will not be exceeded (Ref 11). For air, the gas pressure electrode spacing product is 1 Pa-cm (PASCAL-centimeter). For any pressure spacing product equal to 1 Pa-cm for a voltage of 327 V peak or greater, a glow discharge may occur. Although a glow discharge is not sufficient to cause breakdown, it can initiate the following breakdown sequence:

- 1) Glow discharge;
- 2) The glow discharge will slightly heat the surface causing further outgassing;
- 3) Particulates on the surface will induce surface tracking and eventual breakdown.

With the inverter operating voltages ranging up to 400 Vdc at the input and peak voltage stress of 1 kV at the series capacitors, it is apparent that appropriate high-voltage design practices must be used to prevent destructive corona and arc-overs.

The SRI is expected to operate outside of the corona region, i.e., at pressures close to atmospheric or in the hard vacuum of space at less than 10^{-4} torr. This simplifies the packaging design by allowing for a fully vented packaging approach while using the dielectric properties of air on earth or hard vacuum in space to avoid the electrical failures from voltage breakdown.

The vented design is also the lightest and least costly approach because the alternatives are for void-free dielectric encapsulation with grounded conductive outer surfaces to control voltage stress or to design and maintain a pressurized enclosure with dielectric fluids or gases as the insulating media. Both of these alternative approaches are necessarily more complicated and result in a significant weight increase over the vented packaging approach.

Other considerations for high voltage operation include:

- 1) Applying the usual electrode spacing rules for voltage breakdown in air;
- 2) Selecting dielectric solid materials for encapsulants, and adhesives, insulator bushings, standoffs, wire insulation, and thermal interface dielectrics that have been qualified as low-outgassing materials suitable for sustained operation at 200°C;
- 3) Eliminate or shield all sharp edges on protrusions from conducting surfaces to reduce electrical field stress (screw threads and wire ends are common sources of breakdown so rounded terminal and solder joint configuration should be used);
- 4) Considering nickel plate over aluminum or copper conducting hardware to maximize the voltage breakdown level;
- 5) Positive venting design techniques, including provisions for venting wire bundles, jacketed wire, connectors, stud-mounted parts that tend to entrap air in the clearance spaces, enclosed compartments and the overall housing, because unless specific venting measures are taken throughout the assembly, the desired low-pressure operating region may be unattainable within reasonable time limits;
- 6) Separate low voltage control circuitry from the high-voltage elements using appropriate electrostatic shielding techniques;

- 7) Applying void-free conformal coating on exposed high-voltage conductor surfaces wherever practical to reduce the possibility of surface breakdown from contaminants and electrical assembly debris;
- 8) In using insulation materials, the thickness should keep the maximum voltage stress from exceeding 10% of the actual breakdown voltage (this derating factor is used to account for material properties degradation under long-term voltage stress plus aging effects).

The packaging considerations for high-voltage design stated above are basic for high reliability in the design. Additional factors to consider are to be found in recent NASA and DOD guideline publications on spacecraft high voltage equipment design.

2.7.5 Connectors

Conventional multiwire connectors may be used for control and monitor circuits at the SRI interface but are not advisable for the main power input/output interfaces because of the current density and high voltage considerations. Standard MIL-SPEC connectors are designed with environmentally sealed plug and receptacle elements that entrap air and, in space vacuum, will eventually reach critical pressure causing corona breakdown.

A simpler approach would be to use threaded insulated terminals, sized to handle the current load and fitted with corona suppression caps or cap nuts.

2.7.6 Size and Weight

Using preliminary design data and assumptions on the packaging approach to be used, a size and weight estimate was performed. The results are presented in Table 2.7-2 and represent an estimate considered achievable with present technology for a space-based 200-kW inverter.

Table 2.7-2 Size and Weight Estimates

Components	Weight, kg	Remarks
Thyristor and Diodes	3.6	Vendor Data
Input Filter Capacitors	3.6	Estimate Including Supporting Bracketry
Series Capacitors	1.5	Estimate Including Brackets
Series Inductors	9.0	Assumes Integral Heat Pipe Cooling
av/at Coils	5.0	Estimate Without Heat Pipes
Control and Monitor Circuits	2.0	Estimate
Conductors and Connectors	3.7	Assumes Aluminum Plate and Rod Busing for High-Current Conductors
Subtotal, Electronics	28.4 kg	(62.6 lbs)
Base Structure	11.4	Assumes 50% Solid Structure with Integral Heat Pipes or Coolant Loops
Enclosure	3.6	
Miscellaneous Fasteners	1.3	
Subtotal, Structure	16.3 kg	(35.9 lb)
Radiator	85.0	Assumes 13.9 cm ² (150 ft ²) at 6.1 kg/m ² (1.25 lb/ft ²) Assumes 44 heat pipes at 20 mm diameter and 1.3 m mean length. Includes 3.4 kg for associated cold plates not covered elsewhere. Heat pipe sp. wt. = 0.36 kg/m
Heat Pipes	24.0	
Subtotal, Thermal Control	109.0 kg	(240 lb)
TOTAL SRI SYSTEM WEIGHT	<u>153.7 kg</u>	(339 lb)
Specific Weight at 200 kW	1.7 lb/kW	
<u>Size Estimate</u>		
SRI Assembly	15x46x71 cm (6x18x28 in.)	
Radiator	13.9 m ² (150 ft ²)	

2.8 THERMAL STUDY

The 200-kW dc-dc dual-bridge SRI was studied. The study was limited to the power components and excluded the high-voltage transformer, high-voltage capacitor, and output rectifiers. A 100% duty cycle was assumed. Cold plate requirements at semiconductor interfaces and heat pipes for heat transport were considered.

The power dissipated during operation must be transported away from the electronics and the maximum internal and junction temperatures must be controlled. The ultimate heat sink is deep space and the thermal energy will be transferred to it by radiation. The following assumptions were made:

- 1) A radiator with high emissivity, E greater than 0.95;
- 2) The view factor to space is 1.0;
- 3) Max allowable semiconductor junction temperature is 125°C .

Each diode thyristor pair is estimated to dissipate 625 W. A study was performed to find the radiator area as a function of radiator power dissipation and temperature. The results of this study are shown in Figure 2.8-1. The figure shows that as the radiator temperature increases, for constant power dissipation, the radiator area decreases.

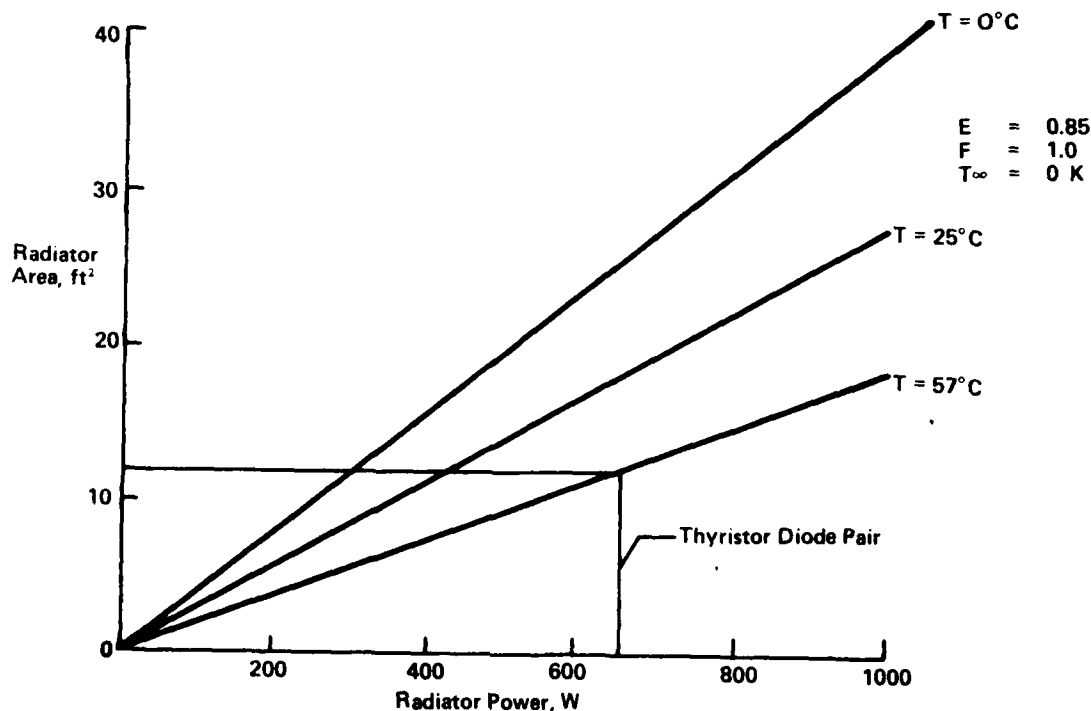


Figure 2.8-1
Radiator Area As a Function of Power Dissipation and Radiator Temperature

Assuming the maximum allowable junction temperature to be 125°C, a typical thermal gradient between the thyristor and radiator is calculated to be 68°C, so the radiator temperature is 125 - 68 = 57°C. For a thyristor diode pair dissipating 625 W and the radiator at 57°C then, approximately 12 ft² of radiator area are required as the figure shows.

The major power dissipators are the thyristor diode pairs--eight pairs, 625 W/pair, or 5000 W total for the eight pairs. Thermal gradients and weight can be minimized by the use of heat pipes. To illustrate the weight savings of using a heat pipe as compared to a solid aluminum conductor, the weight of an aluminum conductor transferring 300 W with a 30°C gradient was calculated and compared to the weight of a heat pipe. Figure 2.8-2 shows the results. For a 30-in. length, the solid aluminum conductor would weigh 200 lbs compared to 3 lb for a heat pipe.

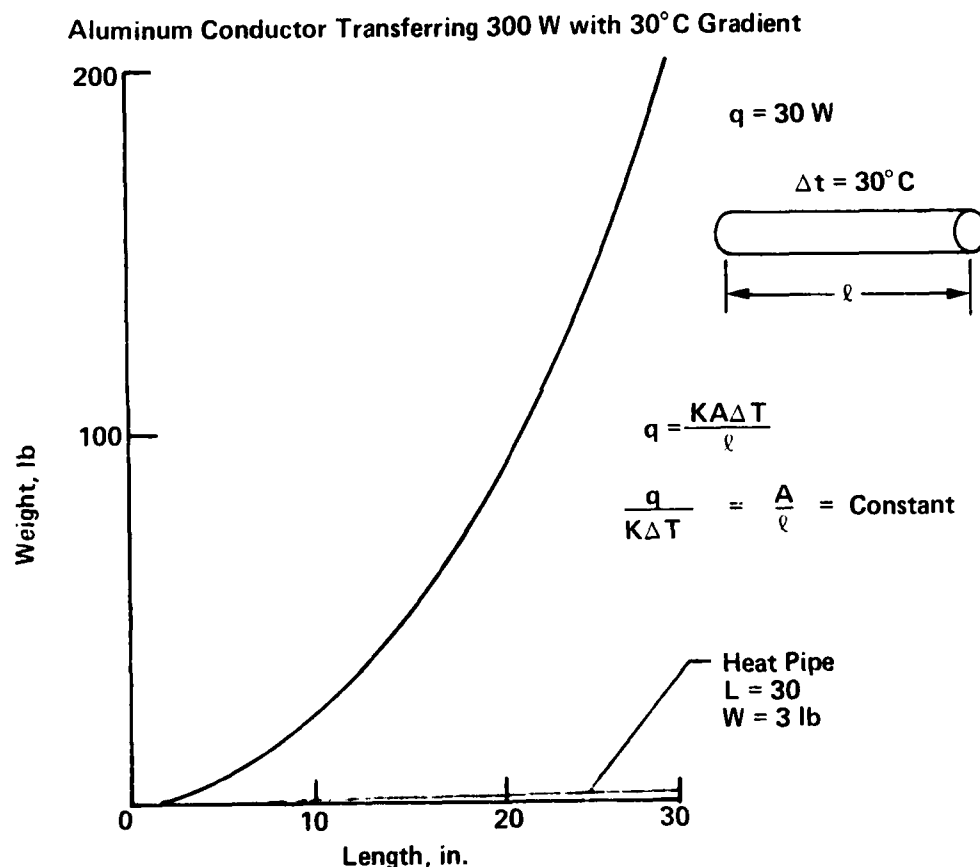


Figure 2.8-2 Aluminum Conductor and Heat Pipe Weights As Function of Length

Figure 2.8-3 shows the thermal configuration of the SCR diode pair. The SCR and diode are connected by the two cold plates. Both sides of the SCR diode pair must be electrically insulated from the heat pipes.

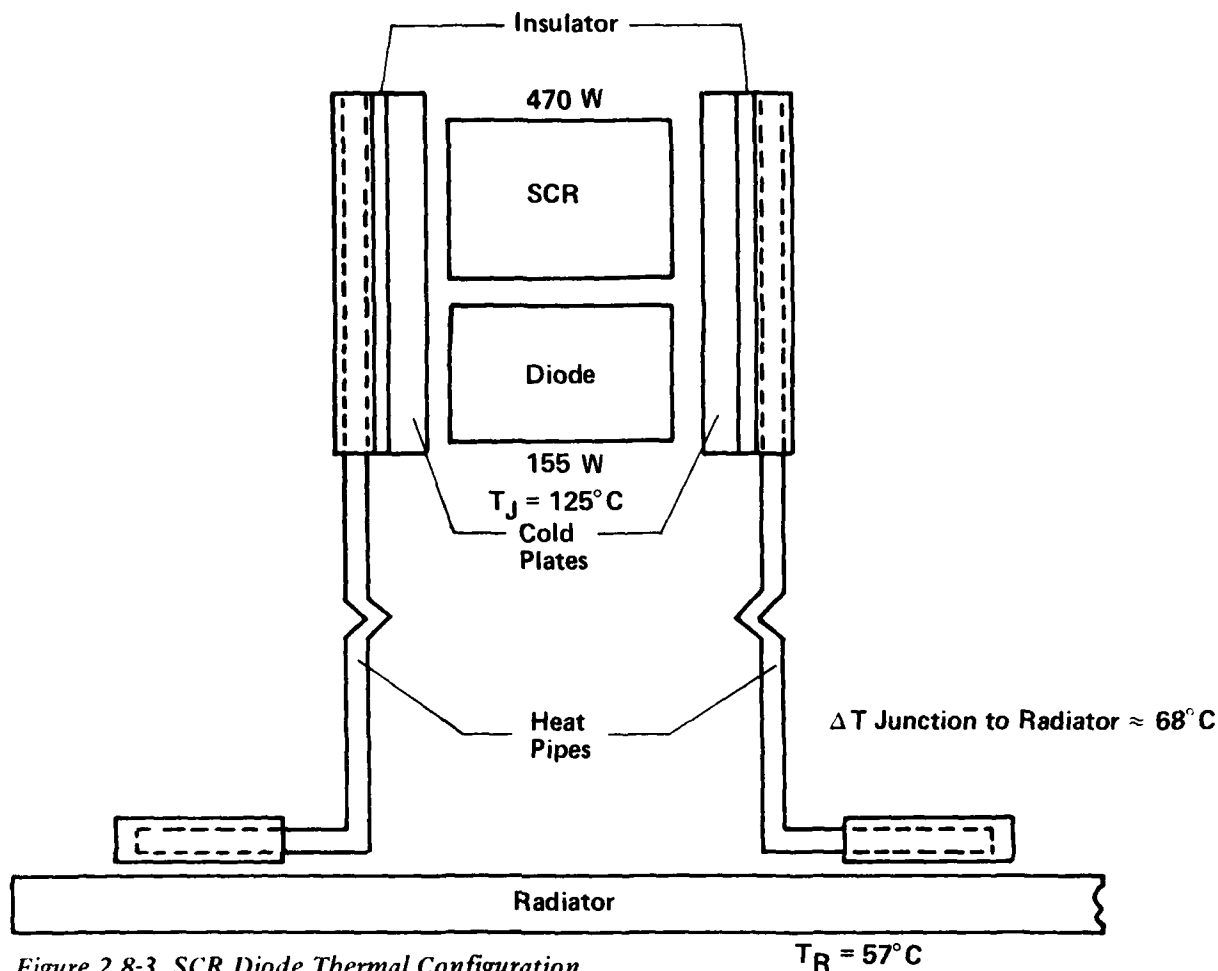


Figure 2.8-3 SCR Diode Thermal Configuration

A parametric study was performed to investigate the relation between radiator temperature, radiator area, and the number of heat pipes for one SCR diode pair. Figure 2.8-4 shows the results. If two heat pipes per pair were used, then the radiator would be at 57°C and each pair would require approximately 12 ft^2 of radiator area. At the other extreme, if nine heat pipes per SCR diode pair were used, or the SCR diode pair were mounted on the radiator, the radiator would be at 87°C and each pair would require approximately 8.3 ft^2 of radiator.

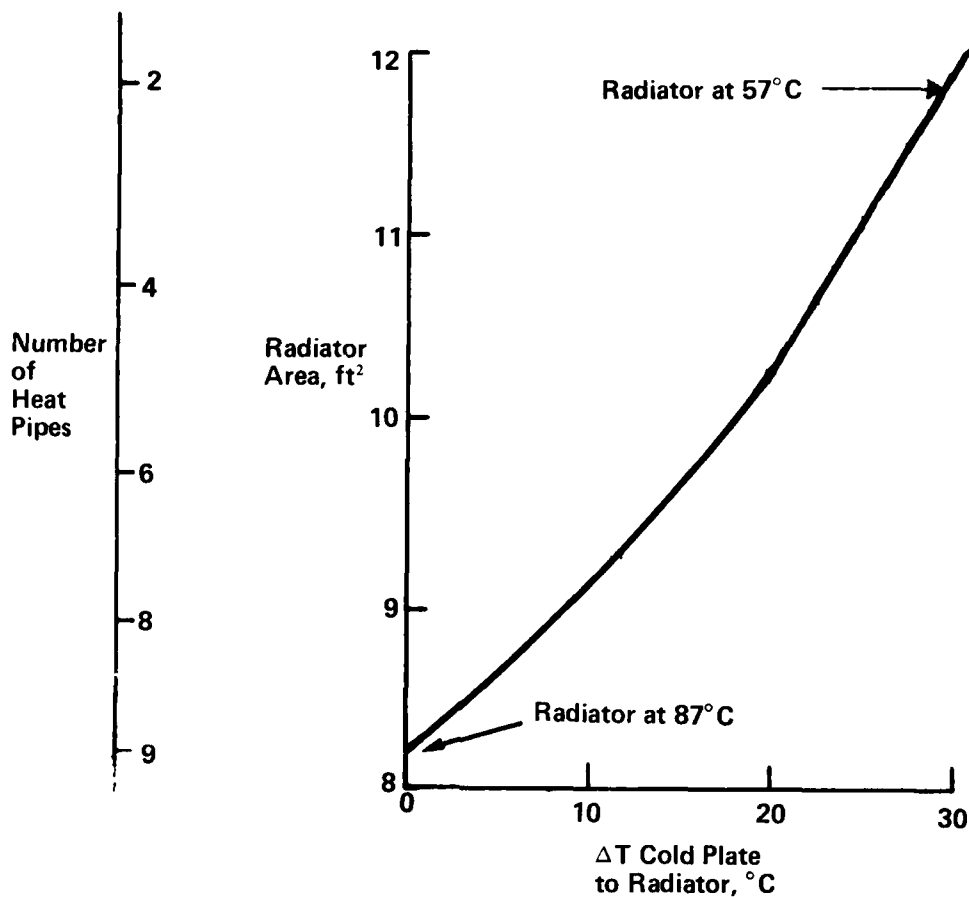


Figure 2.8-4 SCR Diode Thermal Parametric Study

In conclusion, the thermal analysis in this study examined individual parts and determined what is required to maintain the parts within their respective temperature limits.

On a system level the design could be optimized by using several different cold plates in the spacecraft. The different plates should operate at different temperatures and also some plates should be made of electrically nonconductive material. For proper thermal management, the parts should be mounted on the various plates according to their temperature limits and their electrical isolation requirements.

The study showed that for ideal conditions, 150 ft² of radiator area would be required to dissipate 8 kW thermal. As one goes from ideal to a real set of conditions, the required radiator area would be expected to increase.

The analysis also shows that a potential way to reduce the radiator size and spacecraft weight is by using heat pipes to transfer the heat from the cold plates to the radiator. The number of heat pipes per plate should be determined by the desired temperature of cold plate and by the reliability of the heat pipes.

3.0 CONCLUSIONS

From a review of the schematics and breadboards of the three existing APL SRI-based converters, a simplified control and protection architecture was devised that would work with all three of the specified APL SRI-based converter topologies. From conceptual design of the control and protection circuits, it was concluded that they are sufficiently known to justify proceeding to the next phase of the program--detail design, breadboarding, and fabrication and test of the prototype control and protection circuits.

4.0 RECOMMENDATIONS

From the IC technology study, we recommend that the prototype circuits for the back-bias sensor, firing pulse generator, protection unit, and three-phase unit be fabricated with hybrid circuit technology because these circuits have wide application and few external components. We also recommend that the prototype circuit for the control unit be fabricated from discrete components at this time because of the many external components required to customize it to a given power stage topology.

We recommend that CMOS be used for digital circuits because of the low power dissipation, high noise immunity, and availability of radiation-hard equivalents. LM108s and LM111s are recommended for operational amplifiers and comparators because they will meet the electrical requirements of the program and are widely available in both commercial and radiation-hard versions.

The three block diagrams made in the functional design task show the recommended connections of the functional circuits for control and protection of the three SRI power units. The control and protection tasks were grouped into five custom circuits. These custom circuits can be configured to work with all three SRI power units. The five recommended custom circuits are:

- 1) Back-bias sensors;
- 2) Firing pulse generator;
- 3) Protection unit;
- 4) Three-phase unit;
- 5) Control unit.

From the microprocessor study, we recommend that a microprocessor not be incorporated in the present system to reconfigure the prototypes to the different power stages because this is an unproductive use of a microprocessor and would add unnecessary complications. Recommendations are made in the body of the report, however, on possible functions for a microprocessor in a future SRI-based converter.

5.0 LIST OF REFERENCES

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APPENDIX A - RADIATION-HARD MICROPROCESSOR CHIP SETS

Under Mr. Conklin, the Air Force Avionics Lab has played a leading role in pursuing space-qualified development of CMOS/SOS technology. Their work has resulted in what is commonly referred to as the Conklin chip set, or the AFWAL/RCA chip set.

Six device types were of interest in the AFWAL/RCA chip set. Table A-1 summarizes these device types. Three of the device types merit special explanation. The TCS 129 general processing unit (GPU) forms the foundation for the entire chip set. It is an 8-bit-wide ALU slice that can be cascaded to form an arbitrarily wide data word. In addition to shift and complement operations, the GPU can perform ADD, NAND, and OR operations. The TCS 196 is an 8x8-bit two's complement multiplier that can be cascaded to form an NxN multiplier without the use of external logic. This was done by providing partial product logic and signals on the device. The TCS 093 gate universal array (GUA) is used to bind the other devices in the chip set to form a complete system. This large-scale integration (LSI) device eliminates the need for medium-scale integrated (MSI) and small-scale integrated (SSI) circuits. GUAs are fixed regular patterns of transistors and routing paths. By defining the transistor interconnections, GUAs are customized with logic in much the same way read-only memory (ROM) is customized with data.

Table A-1 AFWAL/RCA CMOS/SOS Microprocessor Chip Set

<u>GPU TCS 129</u>		<u>MUL TCS 196</u>	
-	General processing unit	-	8x8-bit multiplier
-	8-bit parallel slice	-	Expandable
-	Concatenatable	-	Completely asynchronous
-	Fully static	-	Latched-input operands
-	125-ns register add		
<u>RAM TCS 246</u>		<u>GUA TCS 093</u>	
-	Random-access memory	-	Gate universal array
-	4k x 1-bit organization	-	-Customized logic
-	125-ns access time	-	632 gate-level complexity
		-	64 pads
-	Read-only memory	-	Proven cell library
-	Fully static 4096 bits	-	100-MHz high-speed divider
		-	452,300, and 182 GUAs also available
-	Mask-programmable		
-	100-ns cycle time	<u>2910 Controllers TCS 158</u>	
		-	Microprogram controller
		-	Functional equivalent to Am2910

The AFWAL/RCA chip set has been implemented in SOS by RCA and by the Center for Radiation-Hardened Microelectronics (CRM) at Sandia Laboratories in their CMOS bulk process.

The AFWAL/RCA chip set has an 8-bit-wide slice architecture. The bit slice architecture requires a large amount of work to produce a working computer, i.e., instruction set definition, microprogramming, and control logic design and reduction to gate arrays. The word length can be 8 bits, or multiples of 8 bits (8, 16, 24, etc). This type of computer will very likely have much more computing power than will be required by a dedicated SRI computer (these are spacecraft central computers, not dedicated power converter microprocessors).

CRM has also produced a radiation-hardened version of an 8-bit microprocessor: Intel 8085 and its peripheral chips. The radiation-hardened version of an Intel 8085 is expected to be much closer to the requirements for a dedicated AIT microprocessor than the bit slice architecture of the AFWAL/RCA chip set.

Table A-2 summarizes the bulk CMOS design constraints.

Table A-2 CRM Radiation-Hard Bulk CMOS Design Constraints

-	Replace N-CH Transmission Gates with Complementary Pairs
-	Replace NOR Logic with NAND
-	Progressive Buffering (Fanout Less Than 4)
-	Eliminate 8-Input NANDS

The CRM Sandia National Laboratories radiation-hardened CMOS microprocessor family has the SA3000 microprocessor (Intel 8085A equivalent). The family also contains hardened CMOS peripheral chips: RAM, ROM, Decoder, CMOS-TTL Level Converter, Bus Transceiver, and I/O Port. A description of the Sandia part numbers and commercial equivalents is in Table A-3. Table A-4 is a summary of the bulk CMOS characteristics.

Table A-3 Radiation-Hardened CMOS Equivalents of Intel 8085A Microprocessor and Support Chips

-	SA3000 Microprocessor (Intel 8085A Equiv)
-	SA3001 RAM I/O-Timer (Intel 8155/56 Equiv)
-	SA3002 ROM I/O (Intel 8355 Equivalent)
-	SA2998 128x8 MNOS RAM
-	SA2999 2Kx8 MNOS EAROM
-	SA2995 3-to-8 Decoder (LS138)
-	SA2996 CMOS-TTL Level Converter (Noninverting CD40116)
-	SA2997 Bus Transceiver (NSC82PC08)
-	SA3025 I/O Port (8212)

Table A-4 Bulk CMOS Technology Characteristics

-	Bulk, P-Well
-	Single Guard Band
-	Projection Lithography
-	Dry Processing for Critical Steps
-	Radiation Hardness $\sim 10^6$ rads (Si)
-	Gate Delay 1 to 4 ns
-	10-V Operation

END

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